GE
Intelligent Platforms

Hardware Reference Manual

CM6
Single/Dual Core PowerPC®
3U CompactPCI® SBC
Fourth Edition

Publication No. HRMCM64E

imagination at work

CM6 Hardware Reference Manual

This manual applies to the CM6 single or dual core MPC8641 3U CompactPCI® Single Board Computer hardware revision 1.0 and above until superseded by a higher revision.

Document History

Edition	Date	By	Chapter	Comments
First	2007-10-29	EH	All	Initial
		HHS	Chapter 7	Correct storage temperature values & styles (non-RoHS)
		HHS	All	Cosmetic changes
		HHS	All	Continued after crash
		EH	All	Adapted for hardware revision 1.x
		EH	All	Implement correctives
		MF	All	Prepared for preliminary release
		EH	Env. cond. Elect. char.	add temp chart RS244/RS485
		HHS	All Page 2	Adjust page breaks Insert new document history table
		HHS	All	Update TOC etc.
		HHS	All	Cleanup minor errors; cosmetic changes
Second	2008-12-15	EH	Chapter 7 Chapter 6	add power and thermal characteristics of CPU types add memory speed restrictions
		HHS	All	Change SBS to GE Intelligent Systems spell-checking
		EH	Chapter 6 PMC Site Compact PCI	add description of the serial auto load EEPROM programming
		HHS	All	Change copyright to 2008; change hidden SBS references
		EH	Real Time Clock	limit the STORE operations to 200k cycles
		HHS	All	Cosmetic changes; change Embedded Systems to Intelligent Platforms in footers
		EH	Env. cond.	add card edge temp for 8-style
		HHS	All	Correct company name; web site address
		HHS	All	Cosmetic changes; correct email addresses; remove Chinese address
		HHS	Ch. 2 & 6	Insert note on NON-transparent operation
Third	2009-03-09	EH	Ch 7	Add curve for single core 1000 MHz low voltage in heat sink diagram
		EH	Ch 7	Add curve for single core 1000 MHz low voltage in heat sink diagram
Fourth	2010-03-30	EH	all	Remove PMC PCI-X capability
		HHS	Ch 4 all	Add info & figure about secondary thermal interface correct footer text; adapt for chapter start on odd pages; change © dates to 2009
		EH	Table 9	Register RSR Bit 4 must be cleared before a new CPU request can be performed

		HHS	Title	Change title & footer to 'Hardware Reference' Manual
		EH		Table 7 and Table 8 pin PMCIO31 added
		EH		Pinout J7002 corrected (PMCIO06/07)
		HHS	All	Change front and rear pages; correct support section
		HHS	All	Correct support chapter; add sales addresses

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GE Intelligent Platforms designs and tests all their products for EMI/EMC conformance. Where GE Intelligent Platforms supplies a complete/functional system for use by end users a certificate will be cited in the manuals/documents which are provided with the products.

Products manufactured by GE Intelligent Platforms should normally be suitable for use in properly designed and produced customer equipment (system boxes or operational systems) without any major redesign or additional filtering. However, the systems might not conform to specific regulations once assembled and used. The system integrator or installer must test for compliance as required in his country or by the intended application and certify this to the end user.

ESD/EMI issues

ESD (Electro-Static Discharge) and EMI (Electro-Magnetic Interference) issues may show up in complete and operational systems. There are many ways to avoid problems with these issues.

Any operational system with cables for I/O signals, connectivity or peripheral devices provides an entry point for ESD and EMI. If GE Intelligent Platforms does not manufacture the complete system, including enclosure and cables, it is the responsibility of the system integrator and end user to protect their system

against potential problems. Filtering, optical isolation, ESD gaskets and other measures might be required at the physical point of entry (enclosure wall of box or rack). For example it is state-of-the-art that protection can not be done at the internal connector of an RTM if a cable is attached and routed outside the enclosure. It has to be done at the physical entry point as specified above.

Products manufactured by GE Intelligent Platforms should normally be suitable for use in properly designed and produced customer equipment (system boxes or operational systems) without any major redesign. However, the systems might be subject to problems and issues once assembled, cabled and used. The end user, system integrator or installer must test for possible problems and in some cases show compliance to local regulations as required in his country or by the intended application.

Corporate addresses

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GE Intelligent Platforms on the Web: http://www.ge-ip.com

For contact and other information (service, warranty, support etc.) see address list in chapter: ‘Support, Service’.

. Welcome

The CM6 CompactPCI Single Board Computer is a PowerPC stand-alone CPU board equipped with numerous functions and add-on features on a minimum board size. This technical manual is designed to provide information regarding the general usage and application of the CM6 CompactPCI Single Board Computer. The hardware design is also outlined.

Chapter 1 gives an overview of the functions, features and devices of the CM6.
Chapter 2 and 3 illustrate unpacking and installation procedures.
Chapter 4 describes all onboard and panel interfaces with pin assignments.
Chapter 5 contains notes on system resources.
Chapter 6 lists details of function blocks.
Chapter 7 outlines electrical, mechanical and environmental specifications.

Appendix A:
The CTM19 transition module is available for the CM6. This board will provide easy access to the rear CM6 interfaces.

Appendix B:
Support, Service and Warranty Information.

Please observe all safety instructions when handling GE Intelligent Platforms products as given in the unpacking and installation chapters.

All documents will be included as files on the Technical Product Information CD-ROM.

Typographic Conventions

This manual uses the following notation conventions:

- *Italics* (sometimes additional in *blue* color) emphasize words in text or documentation or chapter titles or web addresses if underlined.
- Hexadecimal values (base 16) are represented as digits followed by “h”, for example: 0C**h**.

- Hexadecimal values (base 16) are represented as digits preceded by “H”, for example: **H**0C.
- Hexadecimal values (base 16) are represented as digits preceded by “$”, for example: **$**0C.
- Binary values (base 2) are represented as digits followed by “b”, for example 01**b**
- The use of a “#” (hash) suffix to a signal name indicates an active low signal. The signal is either true when it is at logic zero level (voltage close to 0 V) or the signal initiates actions on a high-to-low transition.
- The use of a “\” (backslash) prefix to a signal name indicates an active low signal. The signal is either true when it is at logic zero level (voltage close to 0 V) or the signal initiates actions on a high-to-low transition.
- Text in `Courier` font indicates a command entry or output from a GE Intelligent Platforms embedded PC product using the built-in character set.
- Notes, warning symbols and cautions call attention to essential information.

Product Properties

Certification

The product or products described in this technical manual cannot be operated by themselves. They are components for integration into operational systems or add-ons to such systems. The products have been designed to meet relevant regulatory standards like FCC and CE. As mandated by these standards conformance to these standards can only be certified for complete operational systems. This has to be done by the end-user or by the systems integrator in their operational systems. GE Intelligent Platforms have tested some products in their own systems. Upon request information is available which products have been tested and about the specific environment under which GE Intelligent Platforms has tested these components.

Altitude

Altitude, air pressure and ambient temperature influence the thermal operation of the components described in this manual. They have been developed and tested at about 500 m (1650 ft.) above sea level at a typical ambient temperature of 20 °C (68 °F). Because of only marginal variations within a limited range of altitudes these products operate as specified within altitudes from sea level to 1000 m (3300 ft.). GE Intelligent Platforms can assist the user of these components in planning operation outside this altitude range upon request.

Options

This manual describes the basic product plus all options. Your product may not have all options implemented. Please verify with your purchase contract which options are implemented. Descriptions of options which are not implemented obviously do not apply to your product.

Support, Service and Warranty

The manufacturer grants the original purchaser of GE Intelligent Platforms products a warranty of 24 months from the date of delivery. For details regarding this warranty refer to Terms & Conditions of the initial sale.

Please see chapter “Support, Service, and Warranty Information” on page 84 for further details on repairs and product support.

For support on the web and product information, visit our website at http://www.ge-ip.com

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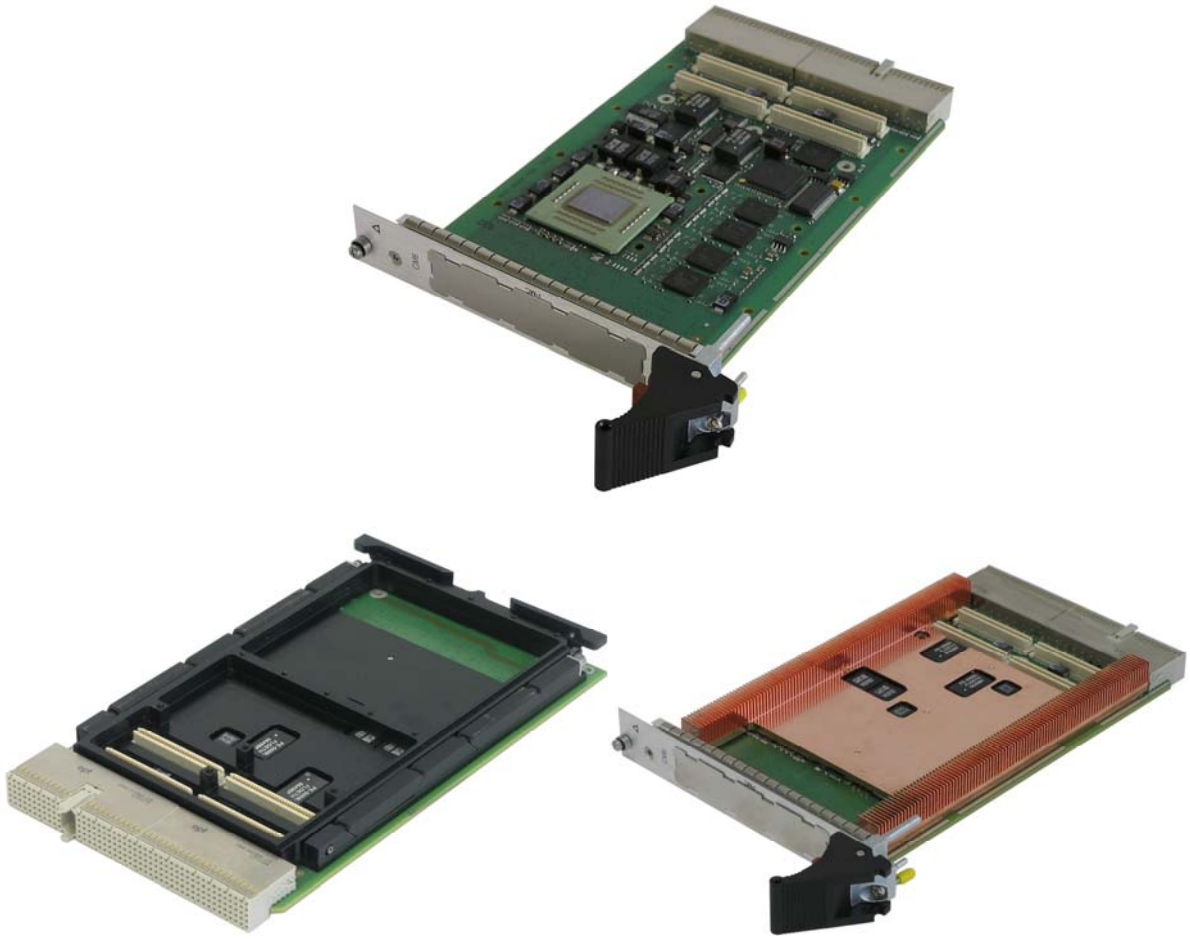

Figure 1: CM6 board versions

Board Design

The SBC (Single Board Computer) CM6 is a PowerPC with single/dual core CPU. It is equipped with many functions a conventional SBC can only offer with several add-on cards. The CM6 offers configurations for either convection cooled or conduction cooled environment. Extension boards can be connected via the CPCI interface and/or PMC interface. The minimized board size and the number of interfaces and functions allow the CM6 to be used in many applications. See the following block diagram for the board design.

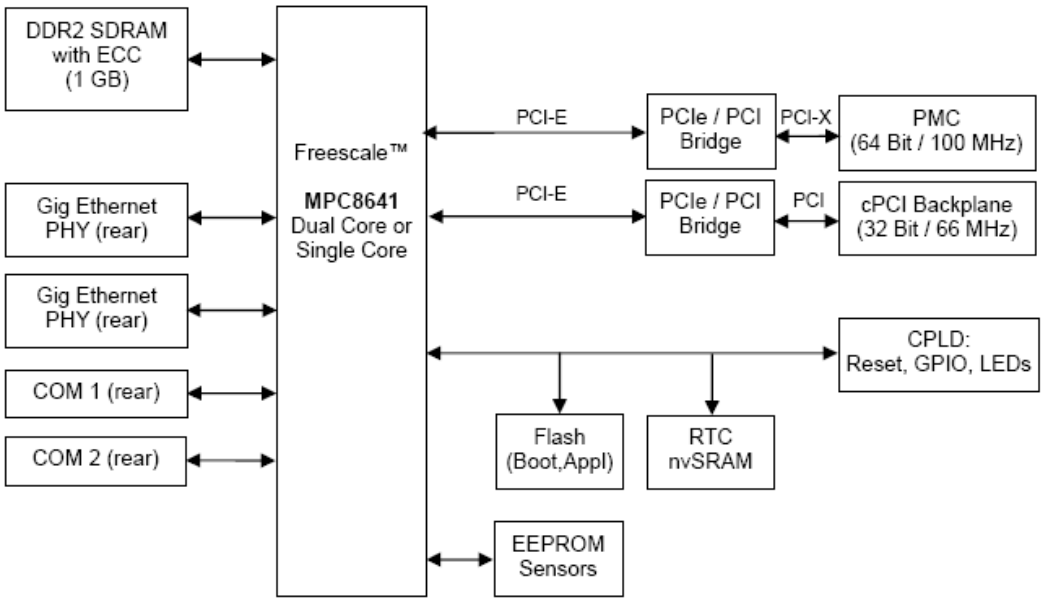

Figure 2: Block diagram of CM6

Design Features

The CM6 CompactPCI Single Board Computer features:

Microprocessor

Single or dual e600 core Freescale® PowerPC™ MPC8641
On-chip 32 Kbytes instruction + 32 kBytes data first level cache
On-chip 1Mbyte second level cache integrated
Integrated system logic required for networking, storage and general purpose embedded applications.
Freescale® single core PowerPC™ MPC8641 processor 1000 MHz-1500 MHz
Freescale® dual core PowerPC™ MPC8641D processor 1000 MHz-1333 MHz

DRAM

DDR2 memory controller with one bank,

512 MByte, 1 GByte, 2 GByte (future) DDR2 SDRAM,
memory interface with up to 333 MHz memory frequency and 667 MHz data rate (depending from used CPU and environment condition)
Each memory bank is ECC controlled and on-board soldered

NVRAM
NVRAM build with a 1 Mbit Serial EEPROM via the SMBus

Flash
Up to 128 MByte (future 256 MByte) Flash which includes a Boot Program,
Flash devices write protected by software or hardware jumper

System Controller
Integrated in MPC8641
Internal CPU MPX bus up to 333MHz
DDR2 SDRAM Controller supports up to 4 Gbit devices
Two PCI Express interfaces
Local Bus interface to external devices
Two integrated Gigabit Ethernet MAC controllers
Two DUART 4-wire interfaces

NVSRAM/Real Time Clock
128kByte non-volatile SRAM and RTC device (max 200k STORE operations)
RTC has no external power back-up and will loose time and date after power off

Watchdog
Two stage Watchdog with interrupt and reset

Timer/Counter
8 timers each 32-bit wide for system timing and periodic interrupt

PMC slot
One 64-bit 66MHz PCI mezzanine slot for standard PMC as well as for rugged PMC. Part of PMC IO signals available at the rear connectors.

Ethernet
Two Gigabit Ethernet ports at rear

Serial IO
Two serial channels each has a 4-wire interface
COM1 with RS232 driver
COM2 with RS422/485 driver

General Purpose IO
8-bit general purpose IOs individually programmable for input, output and triggered interrupt
IO signals are available at rear IO (alternative with PMC IO)

CPCI bus
Compact PCI Bus with PCIe/PCI Bridge Pericom PI7C9X110
PICMG 2.0 R3.0 complaint CPCI local bus standard, 32 bit interface for up to 7 slots at 33 MHz or 4 peripheral slots at 66 MHz
Standard 3U backplanes can be used

Onboard Pull-up resistors are optimized for 3.3 V I/O voltage, but 5 V I/O can also be used for 33 MHz

System/non-System
The CM6 board can be used either as system or peripheral board at the cPCI bus

COP Interfaces
Processor debug interface for external emulator at rear

JTAG Interface
JTAG interface for all devices with JTAG interface accessible at the cPCI connector

Flash Kill
Optional the user can destroy the Flash devices and its content for security reasons (contact factory)

Strapping Configurations
Strapping configurations are available from rear
Hardware write-protection for all programmable devices
Software configuration select
Flash kill option

Required Power Voltages
+3.3 V, +5 V
+12 V and -12 V for supply for PMC modules
+12 V for Flash Kill option

Conduction Cooling
Conduction Cooling available

Conformal Coating
The board can optionally be conformal coated to protect against humidity and fungus devices, configuration selection

LED Indicators
CPU Fail LEDs at rear. Status and user LED at board for debugging

Temperature Sensors
Temperature sensor (LM86) show the temperature of the system board near CPU and CPU die temperature
CPU voltage is shut-off when die temperature reaches 110 °C or board temperature reaches 95 °C

Front Panel
Front panel with PMC opening

Backpanel IO
COM1-2, GPIO[1)], Reset, PMC IO [1)],
2x Gigabit Ethernet, Boot Select, HW Write Protect, Flash Kill[1)], COP
Transition module CTM19 available for compatible connectors
[1)] depends on PMC IO configuration

Approvals

Designed to meet UL (PCB has 94V-0, Self-extinguishing within 10 seconds, no flame drips which ignite)

CHAPTER 2 Unpacking and Inspection

Chapter Scope

This chapter covers the suggested inspection and preparation considerations and background information necessary prior to using the CM6. Unpacking, initial inspection and first-time operation of the CM6 are covered. Following the procedures given in this chapter is recommended, since they will verify proper operation after shipping and before the product is integrated into your system.

ESD

Electrostatic Discharge Notice

The discharge of static electricity, known as Electro Static Discharge or ESD, is a major cause of electronic component failure. The CM6 has been packed in a static-safe bag which protects the board from ESD while the board is in the bag. Before removing the CM6 or any other electronic product from its static-safe bag, be prepared to handle it in a static-safe environment.

You should wear a properly functioning anti static strap and ensure you are fully grounded. Any surface upon which you place the unprotected CM6 should be static-safe, usually facilitated by the use of anti static mats. From the time the board is removed from the anti static bag until it is in the card cage and functioning properly, extreme care should be taken to avoid ‘zapping’ the board with ESD. You should be aware that you could ‘zap’ the board without you knowing it; a small discharge, imperceptible to the eye and touch, can often be

enough to damage electronic components. Extra caution should be taken in cold and dry weather when static easily builds up.

Unpacking and Handling

Although the CM6 is carefully packaged against the rigors of shipping, it is still possible that shipping damages can occur. Careful inspection of the shipping carton should reveal some information about how the package was handled by the shipping service. If evidence of damage or rough handling is found, you should notify the shipping service and GE Intelligent Platforms as soon as possible.

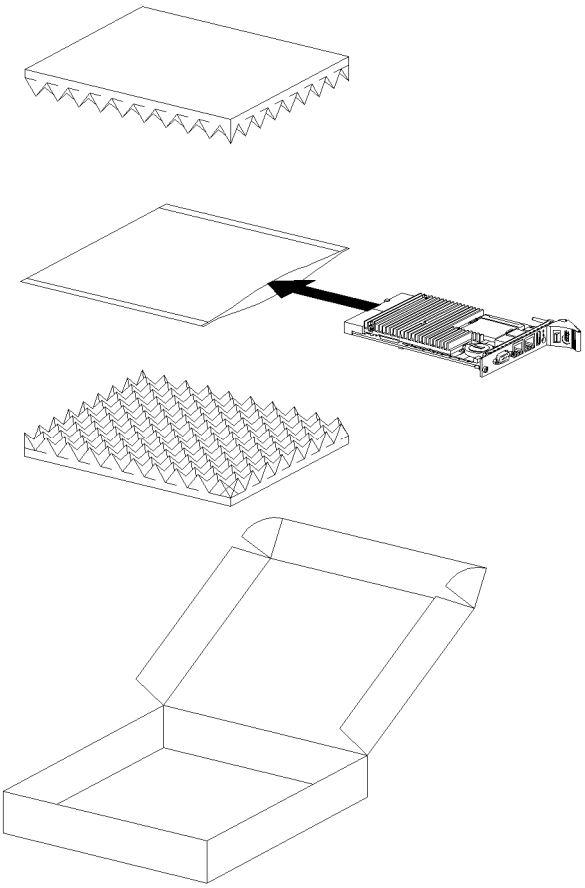

Figure 3: Packaging Material

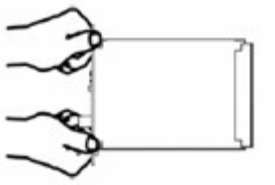

Figure 4: Board handling

Retain all packing material in case of future need.
Only after ensuring that both you and the surrounding area are protected from ESD, carefully remove the CM6 from the shipping carton by grasping it by the front panel and the connectors. Place the board, in its anti static bag, flat down on a suitable surface. You may then remove the board from the anti static bag by tearing the ESD warning labels.

Proper handling of the CM6 is critical to ensure proper operation and long-term reliability. When unpacking the board, and whenever handling it thereafter, be sure to hold the board by the front panel or the card ejectors as shown in the drawing on the left. Do not hold the board by the circuit card edges, the heat sink, or the connectors.

Initial Inspection

After unpacking the CM6, you should inspect it for visible damage that could have occurred during shipping or unpacking. If damage is observed (usually in the form of bent component leads or loose socketed components), contact GE Intelligent Platforms for additional instructions. Depending on the severity of the damage, it may need to be returned to the factory for repair**. DO NOT apply power to the board if it has visible damage.** Doing so may cause further, possibly irreparable damage, as well as introduce a fire or shock hazard.

Attention:

Do not insert a CM6 board in a 3/6U 64-bit Backplane because this may damage electrical interfaces at the CM6.

Please take care that the CM6 is configured for use as a CompactPCI controller in delivery state (CPCI bridge in transparent mode).

For use as a peripheral board (CPCI bridge in NON-transparent mode) please insert the CM6 into a CPCI system slot, power it on and reconfigure the CPCI bridge with the U-Boot command 'bridge':

```
bridge cpci program default peripheral.
```

Delivery Volume

Please check that the delivered package contains the following items:

Table 1: Delivery volume

Qty.	Item	Purpose
1	CM6	CompactPCI Single Board Computer
1	CDROM	Technical Product Information with driver software and manuals in Adobe Acrobat (PDF) format

The manual files are also available through the World Wide Web from our web server:
http://www.ge-ip.com

Available Accessories

The following table lists accessory options which are available for the CM6:

Table 2: Accessory options for CM6

Item	Purpose
CTM19	Transition module, 3U x 4HP

Please contact the sales department or your sales representative for latest information on options and accessories.

Accessories are subject to change without notice.

CHAPTER 3 Installation

Chapter Scope

This chapter covers the installation of the CM6 CompactPCI Single Board Computer in a CompactPCI backplane and initial power-on operations.

General advice

Please observe all safety procedures to avoid damaging system and protect operators and users.

Unpacking and Handling

Please read the manual carefully before unpacking the module or fitting the device into your system. Also adhere to the following:

- Observe all precautions for electrostatic sensitive modules
- If the product contains batteries, please do not place the board on conductive surfaces, anti-static plastic, or sponge, which can cause shots and lead to battery or board trace damage.
- Please do not exceed the specified operational temperatures. Note that batteries and storage devices might also have temperature restrictions.
- Keep all original packaging material for future storage or warranty shipments of the board.

ESD

Electrostatic Discharge (ESD) is a major cause of electronic component failure. The CM6 has been packed in a static-safe bag which protects the board from ESD while the board is in the bag. From the time the board is removed from the anti static bag until it is properly mounted in a backplane, extreme care should be taken to avoid damaging board through electrostatic discharges. See page 25 for details on how to prevent 'zapping' the board with ESD.

General Advisories

Before installing or removing any board, please ensure that the system power and external supplies have been turned off.

Check that jumpers and piggybacks are correctly configured for your application. Mount the board, piggyback, or transition module very carefully. See also sections on additional advisories below.

Do not restore power until you are sure that all modules are fitted correctly and all connections have been made properly.

Advisories for CompactPCI products

Mount the CPU board carefully in the CPCI bus slot. Note that on some boards connectors are used for I/O purposes which must not be inserted into a CPCI bus backplane. A transition module must be used instead.

Minimum System Requirements

As shipped, the CM6 has been thoroughly tested, and is nearly ready for use in your system. In order to verify CM6 operation for the first time, it is suggested that you only configure a minimal system

Because the CM6 is available in several options the description in this chapter is related to the standard configuration.

The following items are required to start the CM6 in a standard configuration:

Backplane and Power Supply

You will need a standard 3U 32bit CompactPCI backplane wired into a regulated power supply capable of providing stable low noise +5 V and +3.3 V sources. Make sure that the supply is capable of meeting the total power requirements of the CM6. Please refer to chapter “Specifications” on page 65 for details.

Initially, you have to plug the CM6 into your 3U system slot of your CPCI system. Please make sure that you do not have the power supply turned ON when the CM6 is plugged into your backplane.

The CTM19 is a 3U x 80 mm rear I/O module which has to be plugged into the CM6 with the backplane between.

Installation

Attention:

Do not insert a CM6 board in a 3/6U 64-bit Backplane because this may damage electrical interfaces at the CM6.

After making sure that you have installed the CM6 properly into your CPCI backplane, connect a VT102 terminal at COM1 (use CTM19) and set the terminal to 115200 baud rate, 8-bit, non-parity. When the board is completely reset the status LED at the board is off and will be set to green by the boot loader at start.

When the processor should begin executing initial boot loader resident routines and when the boot loader is complete the board status LED at the transition module is switched off.

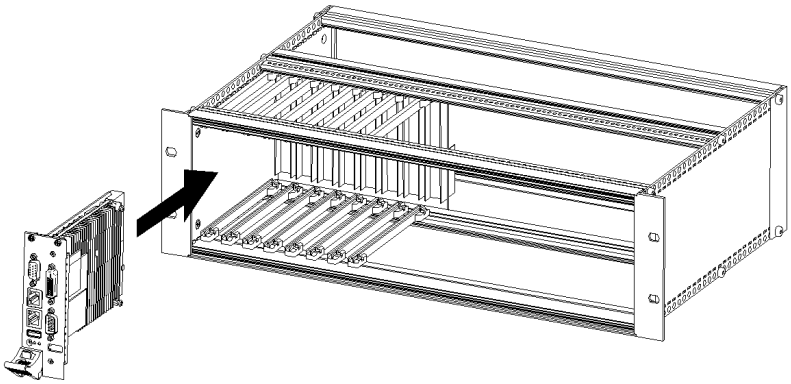

Figure 5: Board in card cage

Please see chapter “Interfaces” for details on onboard interfaces. The location of the CM6 interfaces is shown on page 33.

Initial Power-On Operation

After a few seconds, the CM6 system boot message will appear on the terminal and the status LED is set to green.

If you have seen all the messages so far, you can be confident that the board is running properly and is ready to be installed and setup for your application.

CHAPTER 4 Interfaces

Chapter Scope

This chapter describes the interfaces of the CM6 CompactPCI Single Board Computer located on the board and on the front panel. Each section on a particular interface includes a graphics illustration of the connector and a pin assignment table as well as notes on certain signal line characteristics, if necessary.

For interfaces of the transition module, please refer to the appropriate chapters found in the “Appendices” to this manual.

Figure 6: Board photo

Front Panel Interfaces

Refer to figure 7 for front panel of the CM6 board.

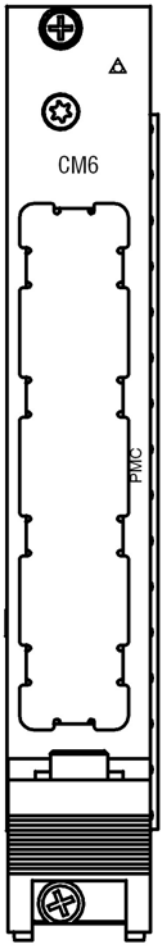

Figure 7: CM6 front panel

CM6 Connectors

This chapter describes connector pin assignments on the CM6. A pin assignment description for available transition module can be found in the corresponding appendix chapters.

CPCI connector reference

The CPCI specification numbers the CPCI connectors from bottom to top J1, J2. The CPCI connectors on the CM6 are J7001and J7001 respectively.

Table 3: CM6 connectors

Signal groups	Pin description
COM1, COM2 signals	C1_..., C2_...
General Purpose I/O	GPIO…
PMC I/O signals	PMCIO…
External Reset Input	PRST#
COP Debug Interface	COP_...
LAN Port A and LAN Port B	LPA_..; LPB_...
Signals separated by a slash	Alternative signal assignments
NC	not connected

Attention:

Do not insert a CM6 board in a 3/6U 64-bit Backplane because this may damage electrical interfaces at the CM6.

CompactPCI bus Connector J7001 and J7002

This interface is used for connection to a standard CPCI backplane.

Table 4: CPCI connectors J7001 and J7002

J7002	A	B	C	D	E	F
22	GA4	GA3	GA2	GA1	GA0	GND
21	CLK6	GND	COP_TDI	SW_CFG#	HW_WP#	GND
20	CLK5	GND	COP_TMS	COP_TRST#	COP_TCK	GND
19	GND	GND	CKSTPIN#	CKSTPOUT	BFAIL#	GND
18	PMCIO03/GPIO2	PMCIO02/GPIO1	PMCIO01/GPIO0	COP_TDO	COP_SRST#	GND
17	PMCIO05/GPIO4	PMCIO04/GPIO3	PRST#	REQ6#	GNT6#	GND
16	PMCIO07/GPIO6	PMCIO06/GPIO5	DEG#	GND	COP_HRST#	GND
15	PMCIO09/FKILL#	PMCIO08/GPIO7	FAL#	REQ5#	GNT5#	GND
14	PMCIO12	PMCIO11	PMCIO10	C1_RXD	C1_RTS	GND
13	PMCIO15	PMCIO14	PMCIO13	C1_TXD	C2_RTS+	GND
12	PMCIO18	PMCIO17	PMCIO16	C1_CTS	C2_RTS-	GND
11	PMCIO21	PMCIO20	PMCIO19	LPB_DA+	LPB_DB+	GND
10	PMCIO24	PMCIO23	PMCIO22	LPB_DA-	LPB_DB-	GND
9	PMCIO26/52	PMCIO25	C2_CTS+	LPB_DC+	LPB_DD+	GND
8	PMCIO28	PMCIO27	C2_CTS-	LPB_DC-	LPB_DD-	GND
7	PMCIO30/37	PMCIO29	C2_TXD+	LPA_DB+	LPA_DA+	GND
6	PMCIO32/39	PMCIO31	C2_TXD-	LPA_DB-	LPA_DA-	GND
5	PMCIO38/44	PMCIO36/42	C2_RXD+	LPA_DD+	LPA_DC+	GND
4	VIO [b]	PMCIO50	C2_RXD-	LPA_DD-	LPA_DC-	GND
3	CLK4	GND	GNT3#	REQ4#	GNT4#	GND
2	CLK2	CLK3	SYSEN#	GNT2#	REQ3#	GND
1	CLK1	GND	REQ1#	GNT1#	REQ2#	GND
J7001	A	B	C	D	E	F
25	+5 V	REQ64# [a]	ENUM#	+3.3 V	+5 V	GND
24	AD01	+5 V	VIO [b]	AD00	ACK64# [a]	GND
23	+3.3 V	AD04	AD03	+5 V	AD02	GND
22	AD07	GND	+3.3 V	AD06	AD05	GND
21	+3.3 V	AD09	AD08	M66EN	C/BE0#	GND
20	AD12	GND	VIO [b]	AD11	AD10	GND
19	+3.3 V	AD15	AD14	GND	AD13	GND
18	SERR#	GND	+3.3 V	PAR	C/BE1#	GND
17	+3.3 V	reserved	reserved	GND	PERR#	GND
16	DEVSEL#	GND	VIO [b]	STOP#	LOCK#	GND
15	+3.3 V	FRAME#	IRDY#	BDSEL#	TRDY#	GND
12-14	KEY	KEY	KEY	KEY	KEY	KEY
11	AD18	AD17	AD16	GND	C/BE2#	GND
10	AD21	GND	+3.3 V	AD20	AD19	GND
9	C/BE3#	IDSEL	AD23	GND	AD22	GND
8	AD26	GND	VIO [b]	AD25	AD24	GND
7	AD30	AD29	AD28	GND	AD27	GND
6	REQ0#	PCIPRESENT#	+3.3 V	CLK0	AD31	GND
5	reserved	reserved	RST#	GND	GNT0#	GND
4	reserved	GND	VIO [b]	reserved	reserved	GND
3	INTA#	INTB#	INTC#	+5 V	INTD#	GND
2	TCK	+5 V	TMS	TDO	TDI	GND
1	+5 V	-12V	TRST#	+12V	+5 V	GND

[a] These signals are not used on the CM6, but have a pull-up to VIO

[b] The VIO signals are either 5 V or 3.3 V, depending on backplane

Reserved – Pin is reserved in the PICMG 2.0 specification. It is not used on the CM6 board

PMC Connectors J7101, J7102, J7103 and J7104

The following table lists the pin assignments of the onboard PMC connector. The PMC slot is PCI 64 bit and 66 MHz capable and works with the internal PCI-PCIe bridge Pericom Pi7C9X130. The PMC is electrical and mechanical compliant to the specification IEEE 1386 and 1386.1 with enhancements of the Processor PMC Standard VITA 32-2003. The enhancements provide pins for a second device (IDSELB and REQB#/GNTB#) and support non-monarch processor PMC cards.

The PCI signaling voltage V(I/O) at the PMC is fixed to 3.3 V but the CM6 PMC is tolerant to 5 V signaling, too.

Secondary Thermal Interface

On conduction-cooled versions of boards and mezzanines the PMC modules may be equipped with optional Secondary Thermal Interfaces. If the PMCs do not fit into their sockets on the CM6 base board then you can remove them. Use a matching TORX screw driver to remove the Secodary Thermal Interfaces. For mounting use a torque of 0.3 Nm to fix the screws or use minimum force to tighten the screws. Add only a short turn (~1/16th) when the screw starts to get tight.

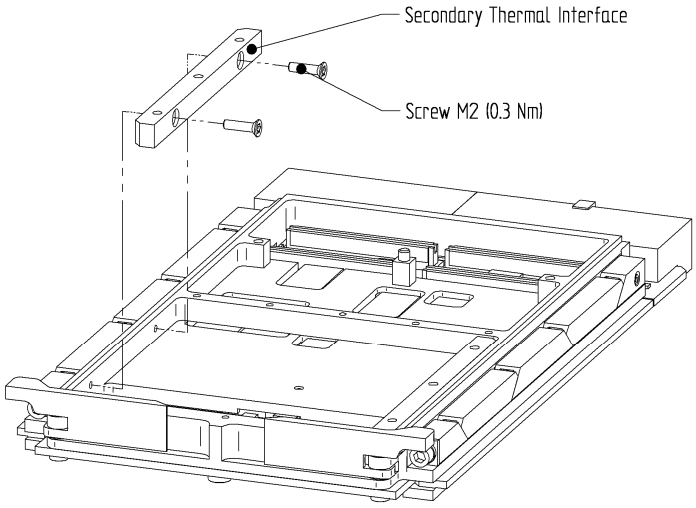

Figure 8: Mounting of Secondary Thermal Interface on PMC module

Table 5: PMC connector pin assignments

P7101	P7102	P7103	Pin	Pin	P7101	P7102	P7103
TCK	+12 V	Reserved	01	02	-12 V	TRST#	GND
GND	TMS	GND	03	04	INTA#	TDO	C/BE7
INTB#	TDI	C/BE6	05	06	INTB#	GND	C/BE5
PRESENT#	GND	C/BE4	07	08	+5 V	Reserved	GND
INTD#	Reserved	V(I/O)	09	10	Reserved	Reserved	PAR64
GND	PUP [a]	AD63	11	12	NC	+3.3 V	AD62
PCICLK	PCIRST#	AD61	13	14	GND	PDN [a]	GND
GND	+3.3 V	GND	15	16	GNT0#	PDN [a]	AD60
REQ0#	PME#	AD59	17	18	+5 V	GND	AD58
V(I/O)	AD30	AD57	19	20	AD31	AD29	GND
AD28	GND	V(I/O)	21	22	AD27	AD26	AD56
AD25	AD24	AD55	23	24	GND	+3.3 V	AD54
GND	AD20 (IDSEL)	AD53	25	26	C/BE3#	AD23	GND
AD22	+3.3 V	GND	27	28	AD21	AD20	AD52
AD19	AD18	AD51	29	30	+5 V	GND	AD50
V(I/O)	AD16	AD49	31	32	AD17	C/BE2#	GND
FRAME#	GND	GND	33	34	GND	AD19 (IDSELB)	AD48
GND	TRDY#	AD47	35	36	IRDY#	+3.3 V	AD46
DEVSEL#	GND	AD45	37	38	+5 V	STOP#	GND
PCIXCAP	PERR#	V(I/O)	39	40	LOCK#	GND	AD44
Reserved	+3.3 V	AD43	41	42	RES.	SERR#	AD42
PAR	C/BE1#	AD41	43	44	GND	GND	GND
V(I/O)	AD14	GND	45	46	AD15	AD13	AD40
AD12	M66EN	AD39	47	48	AD11	AD10	AD38
AD9	AD8	AD37	49	50	+5 V	+3.3 V	GND
GND	AD7	GND	51	52	C/BE0#	REQB#	AD36
AD6	+3.3 V	AD35	53	54	AD5	GNTB#	AD34
AD4	Reserved	AD33	55	56	GND	GND	GND
V(I/O)	EREADY	V(I/O)	57	58	AD3	NC	AD32
AD2	GND	Reserved	59	60	AD1	RSTOUT#	Reserved
AD0	ACK64#	Reserved	61	62	+5 V	+3.3 V	GND
GND	GND	GND	63	64	REQ64#	NC	Reserved

[a] Weak 10kΩ pull-down (PDN) to GND and pull-up (PUP) to VIO.

NC	Not connected
Reserved	Reserved. Do not connect anything
V(I/O)	I/O Voltage, connected with +3.3 V
-12 V/+ 12V	Only available if connected at the CPCI backplane.

Due to the limited rear I/O pins not all 64 PMCIO signals are routed.

Table 6: P7104 connector pin assignments

Pin	P7104 (Pn4)		Pin
01	PMCIO01*	PMCIO02*	02
03	PMCIO03*	PMCIO04*	04
05	PMCIO05*	PMCIO06*	06
07	PMCIO07*	PMCIO08*	08
09	PMCIO09*	PMCIO10	10
11	PMCIO11	PMCIO12	12
13	PMCIO13	PMCIO14	14
15	PMCIO15	PMCIO16	16
17	PMCIO17	PMCIO18	18
19	PMCIO19	PMCIO20	20
21	PMCIO21	PMCIO22	22
23	PMCIO23	PMCIO24	24
25	PMCIO25	PMCIO26*	26
27	PMCIO27	PMCIO28	28
29	PMCIO29	PMCIO30*	30
31	-	PMCIO32*	32
33	-	-	34
35	-	PMCIO36*	36
37	PMCIO37*	PMCIO38*	38
39	PMCIO39*	-	40
41	-	PMCIO42*	42
43	-	PMCIO44*	44
45	-	-	46
47	-	-	48
49	-	PMCIO50	50
51	-	PMCIO52*	52
53	-	-	54
55	-	-	56
57	-	-	58
59	-	-	60
61	-	-	62
63	-	-	64

* These signals are not in each configuration available at rear cPCI_J2 connector see section below for details.

PMCIO – cPCI_J2 Configuration

Not all possible 64 PMCIO are connected to the rear cPCI_J2 connector. Additional to this restriction some PMCIOs signals are alternative assigned with other PMCIOs or signals. See below the signals which are connected from the PMC connector J4 (P7104) to the cPCI_J2 connector.

Either PMCIO01…08 or GPIO 0...7 are connected to the rear and with FlashKill option PMCIO09 is replaced with flash kill signal (FKILL#).

the table below shows the standard PMCIO – cPCI J2 configuration:

Table 7: P7104/P7002 connectors pin assignments

Pin	P7104 (Pn4)		Pin
01	PMCIO01*	PMCIO02*	02
03	PMCIO03*	PMCIO04*	04
05	PMCIO05*	PMCIO06*	06
07	PMCIO07*	PMCIO08*	08
09	PMCIO09**	PMCIO10	10
11	PMCIO11	PMCIO12	12
13	PMCIO13	PMCIO14	14
15	PMCIO15	PMCIO16	16
17	PMCIO17	PMCIO18	18
19	PMCIO19	PMCIO20	20
21	PMCIO21	PMCIO22	22
23	PMCIO23	PMCIO24	24
25	PMCIO25	-	26
27	PMCIO27	PMCIO28	28
29	PMCIO29	PMCIO30	30
31	PMCIO31	PMCIO32	32
33	-	-	34
35	-	PMCIO36	36
37	-	PMCIO38	38
39	-	-	40
41	-	-	42
43	-	-	44
45	-	-	46
47	-	-	48
49	-	PMCIO50	50
51	-	PMCIO52	52
53	-	-	54
55	-	-	56
57	-	-	58
59	-	-	60
61	-	-	62
63	-	-	64

J7002	A	B	C	D	E	F
22	GA4	GA3	GA2	GA1	GA0	GND
21	CLK6	GND	COP_TDI	SW_CFG#	HW_WP#	GND
20	CLK5	GND	COP_TMS	COP_TRST#	COP_TCK	GND
19	GND	GND	CKSTPIN#	CKSTPOUT	BFAIL#	GND
18	PMCIO03*	PMCIO02*	PMCIO01*	COP_TDO	COP_SRST#	GND
17	PMCIO05*	PMCIO04*	PRST#	REQ6#	GNT6#	GND
16	PMCIO06*	PMCIO06*	DEG#	GND	COP_HRST#	GND
15	PMCIO09**	PMCIO08*	FAL#	REQ5#	GNT5#	GND
14	PMCIO12	PMCIO11	PMCIO10	C1_RXD	C1_RTS	GND
13	PMCIO15	PMCIO14	PMCIO13	C1_TXD	C2_RTS+	GND
12	PMCIO18	PMCIO17	PMCIO16	C1_CTS	C2_RTS-	GND
11	PMCIO21	PMCIO20	PMCIO19	LPB_DA+	LPB_DB+	GND
10	PMCIO24	PMCIO23	PMCIO22	LPB_DA-	LPB_DB-	GND
9	PMCIO52	PMCIO25	C2_CTS+	LPB_DC+	LPB_DD+	GND
8	PMCIO28	PMCIO27	C2_CTS-	LPB_DC-	LPB_DD-	GND
7	PMCIO30	PMCIO29	C2_TXD+	LPA_DB+	LPA_DA+	GND
6	PMCIO32	PMCIO31	C2_TXD-	LPA_DB-	LPA_DA-	GND
5	PMCIO38	PMCIO36	C2_RXD+	LPA_DD+	LPA_DC+	GND
4	VIO [b]	PMCIO50	C2_RXD-	LPA_DD-	LPA_DC-	GND
3	CLK4	GND	GNT3#	REQ4#	GNT4#	GND
2	CLK2	CLK3	SYSEN#	GNT2#	REQ3#	GND
1	CLK1	GND	REQ1#	GNT1#	REQ2#	GND

Note
*PMCIO01…08 will be replaced with GPIO 0...7 at option with available GPIOs

Note
**PMCIO09 will be replaced with flash kill signal (FKILL#) option.

PMCIO Configuration:
There is an option available which is optimized for the G2 Graphic PMC card from GE Intelligent Platforms.

Table 8: P7104/P7002 connectors pin assignments

Pin	P7104 (Pn4)		Pin
01	PMCIO01*	PMCIO02*	02
03	PMCIO03*	PMCIO04*	04
05	PMCIO05*	PMCIO06*	06
07	PMCIO07*	PMCIO08*	08
09	PMCIO09**	PMCIO10	10
11	PMCIO11	PMCIO12	12
13	PMCIO13	PMCIO14	14
15	PMCIO15	PMCIO16	16
17	PMCIO17	PMCIO18	18
19	PMCIO19	PMCIO20	20
21	PMCIO21	PMCIO22	22
23	PMCIO23	PMCIO24	24
25	PMCIO25	PMCIO26	26
27	PMCIO27	PMCIO28	28
29	PMCIO29	-	30
31	PMCIO31	-	32
33	-	-	34
35	-	-	36
37	PMCIO37	-	38
39	PMCIO39	-	40
41	-	PMCIO42	42
43	-	PMCIO44	44
45	-	-	46
47	-	-	48
49	-	PMCIO50	50
51	-	-	52
53	-	-	54
55	-	-	56
57	-	-	58
59	-	-	60
61	-	-	62
63	-	-	64

J7002	A	B	C	D	E	F
22	GA4	GA3	GA2	GA1	GA0	GND
21	CLK6	GND	COP_TDI	SW_CFG#	HW_WP#	GND
20	CLK5	GND	COP_TMS	COP_TRST#	COP_TCK	GND
19	GND	GND	CKSTPIN#	CKSTPOUT	BFAIL#	GND
18	PMCIO03*	PMCIO02*	PMCIO01*	COP_TDO	COP_SRST#	GND
17	PMCIO05*	PMCIO04*	PRST#	REQ6#	GNT6#	GND
16	PMCIO06*	PMCIO06*	DEG#	GND	COP_HRST#	GND
15	PMCIO09**	PMCIO08*	FAL#	REQ5#	GNT5#	GND
14	PMCIO12	PMCIO11	PMCIO10	C1_RXD	C1_RTS	GND
13	PMCIO15	PMCIO14	PMCIO13	C1_TXD	C2_RTS+	GND
12	PMCIO18	PMCIO17	PMCIO16	C1_CTS	C2_RTS-	GND
11	PMCIO21	PMCIO20	PMCIO19	LPB_DA+	LPB_DB+	GND
10	PMCIO24	PMCIO23	PMCIO22	LPB_DA-	LPB_DB-	GND
9	PMCIO26	PMCIO25	C2_CTS+	LPB_DC+	LPB_DD+	GND
8	PMCIO28	PMCIO27	C2_CTS-	LPB_DC-	LPB_DD-	GND
7	PMCIO37	PMCIO29	C2_TXD+	LPA_DB+	LPA_DA+	GND
6	PMCIO39	PMCIO31	C2_TXD-	LPA_DB-	LPA_DA-	GND
5	PMCIO44	PMCIO42	C2_RXD+	LPA_DD+	LPA_DC+	GND
4	VIO [b]	PMCIO50	C2_RXD-	LPA_DD-	LPA_DC-	GND
3	CLK4	GND	GNT3#	REQ4#	GNT4#	GND
2	CLK2	CLK3	SYSEN#	GNT2#	REQ3#	GND
1	CLK1	GND	REQ1#	GNT1#	REQ2#	GND

Note
*PMCIO01…08 will replaced with optional GPIO 0...7

Note
**PMCIO09 will replaced with flash kill option (FKILL#)

Transition Module

Please refer to the appendix chapters for interface location and connector pin-outs for the optional transition module CTM19 (Appendix A).

CHAPTER 5 Resources

Chapter Scope

This chapter describes system resources, such as memory mapping, register set and default interrupt request assignments.

Address Map

The MPC8641 supports a flexible 36-bit physical address map. Conceptually, the address map consists of local space and external address space.
The local address map spans 64 GByte. The e600 core uses a 52-bit interim virtual address to address 4 PBytes of virtual memory, and a 36-bit physical address to address 64 GByte of physical memory. The MPC8641 can be made part of an even larger system address space through the mapping of translation windows. This functionality is included in the address translation and mapping units (ATMUs). Both inbound and outbound translation windows are provided. The ATMUs allow the MPC8641 to be part of the larger address maps such as the PCI Express 64-bit address environment.

Local Bus Controller

The local bus controller (LBC) of the MPC8641 in the CM6 is used as a general-purpose machine which supports compatible SRAM, ROM and peripherals with 8-, 16-, 32-bit devices. The supplied chip selects of the LBC are connected to a 32-bit wide boot and application Flash ROM, an 8-bit wide nvSRAM/RTC device and an 8-bit CPLD with CM6 unique status and control registers.
After reset the boot code is fetched from the boot/application Flash ROM. The address map is defined by the boot loader respective depends on the operating system please refer to the appropriate software manual.

CPLD Registers

One device connected at the LBC is the CPLD (U1949) which provides seven CM6 specific control and status registers. The CPLD register are connected to the Local Bus Controller at chip select LCS1 with 8-bit data width. The bit description is in little endian, least significant bit is at the right and most significant bit at the left end of the byte.

Reset Source Register (RSR)

Address: Base + Offset 0
Size: 8 bit

Table 9: Reset Source Register (RSR)

Bit	Name	Write	Read	Default
0	R_PWR	any write clears the bit *	1: last reset caused by voltage monitor	not defined
1	R_THERM	any write clears the bit *	1: last reset caused by power down of the thermal protection	not defined
2	R_PCI	any write clears the bit *	1: 1ast reset caused by Reset button, cPCI Reset (non System only) or RESETOUT# from PMC	not defined
3	reserved	-	0	n/a
4	R_HRSTREQ	any write clears the bit *	1: last reset caused by CPU reset request Must be cleared before a CPU reset request is performed	not defined
5	R_COPRST	any write clears the bit *	1: last reset caused by COP Interface HRESET or SRESET	not defined
6	R_WDGRST	any write clears the bit *	1: last reset caused watchdog circuit	not defined
7	PWR_ON	any write clears the bit *	0 – warm reset 1 – cold reset (power-on)	1 – after power on reset

* Any write to the Reset Source Register clears all bits of this register.

After a power-on cycle all bits of this reset register should be cleared. If afterwards there is an unexpected (or expected) reset the source can be determined by the bits which are set.

Control Register (CR)
Address: Base + Offset 1
Size: 8 bit

Table 10: Control Register (CR)

Bit	Name	Write	Read	Default
0	COM2_DE	0: COM2 RS422/485 driver is disabled 1: COM2 RS422/485 driver is enabled	0: COM2 RS422/485 driver is disabled 1: COM2 RS422/485 driver is enabled	0- driver disabled
1	WP_FLASH	0 – Flash is writeable 1 - Flash is write protected	0 – Flash is writeable 1 - Flash is write protected	1- Flash write protected
2	WP_SPD	0 – SPD EEPROM is writeable 1 - SPD EEPROM is write protected	0 – SPD EEPROM is writeable 1 - SPD EEPROM is write protected	1- SPD EEPROM is write protected
3	WDG_WP	0 – Watchdog Control Register (WCR) is not write protected 1 – Watchdog Control Register (WCR) is write protected	0 – Watchdog Control Register (WCR) is not write protected 1 – Watchdog Control Register (WCR) is write protected	0 – Watchdog Control Register (WCR) is not write protected
4	LED_GREEN	0 - green part off the bi-color LED is off 1- green part of the bi-color LED is on	0 - green part off the bi-color LED is off 1- green part of the bi-color LED is on	0 - green part off the bi-color LED is off
5	LED_RED	0 – red part off the bi-color LED is off 1- red part of the bi-color LED is on	0 - red part off the bi-color LED is off 1- red part of the bi-color LED is on	0 - red part off the bi-color LED is off
6	BOARD_STAT	0 – set the BOARDSTAT output signal to high 1 – set the BOARDSTAT output signal to low	0 – BOARDSTAT output signal is high 1 – BOARDSTAT output signal is low	0 – set the BOARDSTAT output signal to high
7	MASK_SMI	0 – SMI output of PLD is enabled 1 – SMI output is masked and force SMI to inactive	0 – SMI output of PLD is enabled 1 – SMI output is masked and force SMI to inactive	0 - SMI output of PLD is enabled

Status Register 0 (STAT0)
Address: Base + Offset 2
Size: 8 bit

Table 11: Status Register 0 (STAT0)

Bit	Name	Write	Read	Default
0	PMC_M66EN	-	0 – PMC PCI bus 33MHz 1 – PMC PCI bus 66MHz	-
1	CPCI_M66EN	-	0 – CPCI bus 33MHz 1 – CPCI bus 66MHz	-
2	SYSEN	-	0 – CM6 is peripheral (non-system) board 1 – CM6 is system board	-
3	HW_CFG	-	0 – hardware configuration signal HW_CFG# is open 1 – hardware configuration signal HW_CFG# is tied to GND level	-
4	HW_WP	-	0 – hardware configuration signal HW_WP# is open 1 – hardware configuration signal HW_WP# is tied to GND level If signal is active all write operations to flash and nvSRAM devices are inhibited by hardware logic.	-
5	SYSCLK_SEL0		System clock selection bit 0	-
6	SYSCLK_SEL1		System clock selection bit 1 SEL1 SEL0 SYSCLK 0 0 166 MHz 0 1 66 MHz 1 0 100 MHz 1 1 133 MHz	-
7	PMC_PCIXCAP		0 - PMC is in conventional PCI mode 1 – reserved	-

Status Register 1 (STAT1)

Address: Base + Offset 3
Size: 8 bit

Table 12: Status Register 1 (STAT1)

Bit	Name	Write	Read	Default
0	WDG_INT	-	0 – Watchdog Interrupt not active 1 – Watchdog Interrupt active Clear it with Watchdog Trigger (WTIG)	-
1	reserved	-		1
2	reserved	-		1
3	DEG	-	0 – DEG# not active 1 – cPCI backplane signal DEG# indicates the internal temperatures of the system are within 10°C of the thermal shutdown limit. An active DEG signal asserts the SMI (System Management Interrupt) to the CPU.	-
4	FAL	-	0 – FAL# not active 1 – cPCI backplane signal FAL# indicates the system supply has shut off the outputs due to a problem or the input voltage has been switched off. An active FAL signal asserts the SMI to the CPU.	-
5:7	reserved	-	Always 0	-

Watchdog Register (WCR)

Address: Base + Offset 4
Size: 8 bit

Table 13: Watchdog Register (WCR)

Bit	Name	Write	Read	Default
2:0	WINT[2:0]	Set Watchdog Interrupt time	WINT2 WINT1 WINT0 Time 0 0 0 disabled 0 0 1 256ms 0 1 0 512ms 0 1 1 1024ms 1 0 0 2048ms 1 0 1 4096ms 1 1 0 8192ms 1 0 1 16384ms	WINT[2:0]: 001
3	Reserved	-	Always 0	-
6:4	WRST[2:0]	Set Watchdog Reset time	WRST2 WRST1 WRST0 Time 0 0 0 0 ms 0 0 1 256ms 0 1 0 512ms 0 1 1 1024ms 1 0 0 2048ms 1 0 1 4096ms 1 1 0 8192ms 1 0 1 16384ms	WRST[2:0] : 000
7	Reserved	-	Always 0	-

The implemented watchdog has two timer stages the watchdog interrupt (WINT) and the watchdog reset (WRST). The elapsing of the first timer stage (WINT) generates a System Management Interrupt (SMI), and starts the second stage (WRST) of the watchdog and may generate a reset if the selected time of the second stage is elapsed.
The watchdog timers are retriggered by a write to register WTIG and will reset both watchdog stages (WINT and WRST).

The watchdog is disabled if WINT[2:0] = 000. If WRST[2:0] = 000 the reset will be generated at the elapsing time of the WINT watchdog timer.
After power-on the watchdog is active and will perform a reset after 256ms, if no retrigger or disable command is performed.
It is possible to write protect (WDG_WP bit in the Control Register) the Watchdog register (WCR) to prevent unallowed writes.

Watchdog Trigger (WTIG)

Address: Base + Offset 5
Size: 8 bit

Table 14: Watchdog Trigger (WTIG)

Bit	Name	Write	Read	Default
7-0	WTIG	Retrigger watchdog timer	Always 0	-

Any write to this register will reset the Watchdog timers and restart the timers with the selected watchdog time.

Boot Code Register (BCR)

Address: Base + Offset 6
Size: 8 bit

Table 15: Boot Code Register (PCR)

Bit	Name	Write	Read	Default
7-0	PCODE	Boot Code	Last Boot code	0x00

It is possible to write Boot Codes to this register. If this Boot Code has another value than ‘00hex’ and longer stable than two seconds the value is transferred to the red LED (morse code). A long blink is a 1; short blink is 0 starting with bit seven of the actual Boot Code.

PLD Version Register (VER)

Address: Base + Offset 7
Size: 8 bit

Table 16: PLD Version Register (VER)

Bit	Name	Write	Read	Default
7-0	PLD	N/a	PLD Version	-

Status Input Ports

Besides the registers in the CPLD the CM6 provides additional status information at the input ports of the ETSEC1 and ETSEC2 ports of the MPC8641.

The ETSEC1_RXD[7:0] and ETSEC2_RXD[7:0] ports are used as Input ports. For programming see MCP8641 manual.

Table 17: ETSEC1

Port	Name	Read	Default
ETSEC1_RXD[4:0]	GA[4:0]	Geographical Address connected to the GA pins of the cPCI connector	-
ETSEC1_RXD5	PCI_PRESENT	0 – CPCI backplane is present 1 – CPCI backplane is not present	-
ETSEC1_RXD6	PMC_PRESENT	0 – PMC card is present at the slot 1 – PMC card is not present at the slot	-
ETSEC1_RXD7	reserved	-	-

Table 18: ETSEC2

Port	Name	Read	Default
ETSEC2_RXD0	EREADY	0 – PMC card is busy with internal enumeration of the PCI bus 1 – PMC has finished PCI enumeration and is ready for access	-
ETSEC2_RXD1	FLASH_BUSY	0 – Flash devices are busy with a current program or erase command 1 – Flash devices are ready to accept commands	-
ETSEC2_RXD[7:2]	Reserved	-	-

General Purpose I/O Port

The CM6 uses the I/O Port of the PCI-PCIe Bridge Pericom Pi7C9X130 and Pericom Pi7C9X110 for the general purpose I/Os which are optional available at the rear. For programming see the manual of appropriate Pericom bridge

Table 19: GPIO

Name	Write/Read	Default
GPIO[3:0]*	GPIO[3:0] are connected at the Pericom Bridge PI7C9X130 GPIO[3:0]	-
GPIO[7:4]	GPIO[7:4] are connected at the Pericom Bridge PI7C9X110 GPIO[3:0]	-

* GPIO[3:0] are not usable in board revision 1.x

Interrupts

The MPC8641 has a bunch of external interrupts inputs. The list below shows the usage in the CM6.

Table 20: Interrupts

Interrupt	Name	Comment
MCP0	Not used	
MCP1	Not used	
SMI0	WDG/DEG/FAL	Watchdog or Power Supply System Management Interrupt
SMI1	Not used	
IRQ0	INT_PHYA	Alert from Gigabit PhyA
IRQ1	INT_PHYB	Alert from Gigabit PhyB
IRQ2	INT_RTC	RTC Interrupt
IRQ3	Not used	
IRQ4	Not used	
IRQ5	Not used	
IRQ6	Not used	
IRQ7	Not used	
IRQ8	GPIO4	GPIO change interrupt
IRQ9	GPIO5	GPIO change interrupt
IRQ10	GPIO6	GPIO change interrupt
IRQ11	GPIO7	GPIO change interrupt

PCI Busses

The MPC8641 provides two PCI-Express channels. Each of the both channels is connected to a PCIe/PCI bridge.

PCIe channel one is four lane wide and provides with a Pi7C9X130 bridge the 64bit/66MHz PCI for the PMC slot.

PMC: IDSEL (A) AD20
IDSEL (B) AD19

PCIe channel two is one line wide and provides with the Pi7C9X110 bridge the 32bit/66MHz PCI bus for the cPCI compliant backplane. This bridge is a universal transparent/non-transparent bridge to support the CM6 as system slot controller or non-system (peripheral) slot controller function.

SMBusses

The MPC8641 supports two System Management Buses (SMB).

SMBus 1

Bus one is connected to a nonvolatile digital switch device for selecting different power-on reset configurations. Following devices and address scheme are used.

Address:
1010 111x nonvolatile digital switch DS3905

SMBus 2

SMBus two connects the CM6 board specific serial devices. Following devices and address scheme are used.

Address:

1101 110x	clock device ICS9FG104
1001 100x	Thermo Sensor LM86
1010 01xx	User EEPROM 128kByte
1010 00xx	SPD and Factory EEPROM 256Bytes

CHAPTER 6 Function Blocks

Chapter Scope

This section gives a brief overview over the software interfaces of onboard devices on the CM6 CompactPCI Single Board Computer.

Processor

The CM6 is driven by the Freescale MPC8641 processor. This processor integrated either one or two PowerPC e600 cores (previously referred to as the G4 core) with system logic required for networking, storage and general purpose applications. The e600 core consists of a processor core, 32Kbyte separate level-one instruction and data caches and a 1Mbyte L2 cache. The two cores can have private address space without any special software involvement. The high level of integration in the MPC8641 helps simplify board design and offers significant bandwidth and performance increase. The internal MPX processor bus runs with a maximal frequency of 333MHz. The MPC8641 has two memory controllers, a local bus controller, a programmable interrupt controller, two I2C controllers, four channel DMA controller and a dual universal asynchronous receiver transmitter (UART). For high speed interconnect the MPC8641 provides two sets of PCI Express interfaces. The device has also four integrated 10/100/1000 Ethernet controllers.

Clock Assignment

The clock scheme of the CM6 is very flexible. The main clock is a generated from PLL and support 66MHz, 100MHz, 133MHz, and 166MHz for the MPC8641. With this main clock the MPC8641 determines with configuration pins the ratio between main clock – MPX-, memory, core, local bus-clock. The selected main clock can be read at PLD register STAT0 bit [5:6], and the ratio factors of the MPC8641 in the power-on reset register (PORPLLSR).
Clocks for the PCI Express (100MHz), PCI (33/66/100MHz), Timer (25MHz), and Ethernet controller (125MHz) are supplied separately.
The clock frequency is set at the factory according to the used MPC8641 speed grade.

Memory Controller

The CM6 uses only one of the two memory controllers in the MPC8641. CM6 supports double data rate 2 synchronous DRAM (DDR2 SDRAM) up to a clock rate of 333 MHz (data rate of 667MHz) and a data bus width of 64 bits, this is equivalent to the PC2-5300 specification (5.3Gbyte/s bandwidth). Memory speed depends on used MPC8641 version and environment requirements, please contact factory. One soldered bank is provided by the CM6 with a size of either 512 MByte, 1Gbyte, or 2Gbyte (future). A built-in 8-bit wide error correction code (ECC) ensures the data integrity of the memory bank.

Flash Memory

The CM6 provides one bank of 128MB or 256Mbyte soldered flash ROM. The flash devices are located on Local Bus Controller of the MPC8641 with a 32bit wide data bus. The flash memory holds the boot loader of the CM6 and optional the application software.

Flash Write Protection

Operating software can write and erase data from the flash devices. Each flash device provides 'chip erase' functions as well separate erase and protection of sectors. The CM6 provides several write-protect mechanism to prevent code data loss during power cycling and system initialization.

External Write Protection

The HW_WP# signal at the backplane (J2 pin E21) prevents any write to the flash ROM.
If the HW_WP# signal is asserted (active low) all write commands to the Flash devices are disabled. That means even the command, "Read Device Code" is inhibited.
The state of HW_WP# can be read in the CPLD Configuration Register.

Device Write Protect

Inside the MPC8641 Local Bus Controller register set the according chip select (LCS1) of the Flash Device may set to write protect.

Boot Code Selection

The SW_CFG# signal provided at the backplane (cPCI J2 pin D21) selects which boot code is executed on power-up or reset. If SW_CFG# is inactive (high) the code in the user boot ROM is executed, provided that a boot description header with a valid checksum is detected. If SW_CFG# is active (low) an emergency boot code is executed.

Flash Kill Option

For security reasons the flash devices can be destroyed with this optional feature. If signal FKILL# (cPCI J2 pin A15) is tied to ground the flash devices are supplied with +12 V instead +3.3 V. This over voltage will destroy the devices and its content. In inactive state the signal FKILL# has a high level of +12 V that means an output which drives FKILL# must withstand a high level of +12V. The feature is only usable if the CM6 is supplied with +12 V power rail. Besides the flash devices other logic may be damaged if a Flash Kill is performed!

PCI Express Bus

The MPC8641 includes two PCI Express x1/x2/x4/x8 Buses.

The PCI Express controller connects the internal platform to a 2.5-GHz serial interface. Upon coming out of reset, the PCI Express interface performs link width negotiation and exchanges flow control credits with its link partner. Once link auto negotiation is successful, the controller is in operation.

The CM6 uses both PCI Express Buses for connection of the cPCI and PMC PCI to PCIe bridges. The bus to the PMC bridge is x4 wide and connected to a PCI PCIe bridge (Pericom Pi7C9X130). The second PCI Express bus is connected to the cPCI bridge with an x1 PCIe connection Pericom bridge Pi7C9X110.

PMC Site

The CM6 hosts one single-wide PMC site that includes the following features:
PMC site supports standard IEEE 1386.1 PMC modules. PMC site is located on a 64-bit 33/66 MHz PCI Bus. The mode of operation is determined by the M66EN and PCIXCAP signals. The PMC Bus supports +3.3 V VIO but is +5 V tolerant. PMC_Pn4 I/O signals are partial routed to cPCI_J2.
It can host a PMC module with power ratings of 7.5 W or less.
The PCI bus of the PMC is provided by a PCIe/PCI bridge Pericom PI7C9130.
PMC Bridge Vendor ID: 12D8h
PMC Bridge device ID: E120h
The PMC Bridge has a serial autoload EEPROM which loads at every power-up standard register setting into the bridge. This serial EERPOM is programmed at the factory. It is strongly recommended not to access this device under user software, because irregular content may prevent the board to boot-up.

Compact PCI

The CM6 provides a cPCI compliant 66MHz/32bit PCI bus. The PCI signaling voltage V(I/O) at the cPCI can be either 3.3 V or 5 V. If the signal voltage is 3.3 V the CM6 can tolerate 5 V signaling.

The CM6 cPCI bridge can function as a system controller or a peripheral card; the Pi7C9X110 PCIe/PCI bridge must change the mode and handling of data and PCI signals according to the mode of operation. The mode of operation is selected by the signal SYSEN# (cPCI_J2 pin C2) at the cPCI backplane.
When the CM6 is a system controller the bridge is in transparent mode which means the PCI host looks through the bridge to the backplane and initial and enumerate all devices and peripherals throughout the system.
When the CM6 is peripheral card the bridge is in non-transparent mode which means that it cannot configure past to the backplane.

The system/non-system mode of operation affects how the CM6 handles reset, clocks, interrupts and request/grant signals.

System mode:
- cPCI reset (RST#) is driven (output)

- cPCI clocks (CLK0…CLK6) are driven (outputs)
- PCI interrupts (INTA.D) are inputs and handled by the system
- the cPCI arbitration of the seven REQ/GNT is handled in the system board

Non-System mode:
- cPCI reset (RST#) is input
- cPCI clock (CLK0) is input
- board is a interrupt requester
- board request cPCI bus and must wait until the system board grant the bus

cPCI Bridge Vendor ID: 12D8h
cPCI Bridge device ID: E110h

The cPCI Bridge has a serial autoload EEPROM which loads at every power-up standard register setting into the bridge. The content of the EEPROM differs if the board is used either as system or non-system board. The boot-up program can program the autoload EEPROM device with the correct content in dependence of the current board position. If the content of the EEPROM must be reprogramed the system has to be switched off/on afterwards to load the changed register settings.
It is strongly recommended not to access this device under user software, because irregular content may prevent the board to boot-up.

Please refer to the '**Attention**' paragraph under 'Initial Inspection' in Chapter 2, Unpacking and Handling.

Watchdog

For security of application software, the CM6 offers a software controlled hardware two stage watchdog with independent count values for each stage. First stage generates a SMI. The second stage issuing a reset signal if its time-out interval expires. The configurable granularity reaches from 256 ms to 16384 ms.

For more information please see the watchdog registers in section CPLD Registers.

nvSRAM Real Time Clock

The CM6 provides the Simtek STK17TA8 which combines a 1 Mbit nonvolatile static RAM with a full-featured real-time clock.

The SRAM can be read and written an unlimited number of times, while independent, nonvolatile data resides in the nonvolatile elements. On each power-up/power-down cycle the SRAM is automatically loaded from respectively stored in the nvSRAM part of the chip.

The device provides unlimited load/recall operations but the **STORE operations are limited to 200k.** STORE operation are always performed at power-off cycle or activated by an address sequence.

The Real-Time Clock function provides an accurate clock with leap year tracking and a programmable, high accuracy oscillator. The Alarm function is programmable for one-time alarms or periodic seconds, minutes, hours, or days. There is also a programmable Watchdog Timer for process control.

No backup operation during power-off time is provided to the Real Time Clock, so each time the board is switched on the actual date/time must be reloaded by software.

External Write Protection

The HW_WP# signal at the backplane (J2 pin D21) prevents any write to the nvSRAM/RTC. If the HW_WP# signal is asserted (active low) all write commands to the nvSRAM/RTC device are disabled. That means also the RTC part is write protected. The state of HW_WP# can be read in the CPLD Status Register0 bit 4.

Device Write Protect

Inside the MPC8641 Local Bus Controller register set the according chip select (LCS2) of the Flash Device may set to write protect.

Serial Interface

The CM6 has two serial ports which are provided by the MPC8641 DUART. The DUART consists of two universal asynchronous receiver/transmitters (UARTs). Each UART is clocked by the MPX bus clock. The DUART programming model is compatible with the PC16552D.

The DUART includes these features:

- Full-duplex operation
- Programming model compatible with the original PC16450 UART and the PC16550D (an improved version of the PC16450 that also operates in FIFO mode)
- FIFO mode for both transmitter and receiver, providing 16-byte FIFOs
- Serial data encapsulation and decapsulation with standard asynchronous communication bits (START, STOP, and parity)
- Maskable transmit, receive, line status, and modem status interrupts
- Software-programmable baud generators that divide the MPX clock by 1 to $(2^{16} - 1)$
- Clear to send (CTS) and ready to send (RTS) modem control functions
- Line and modem status registers
- Line-break detection and generation
- Internal diagnostic support, local loopback, and break functions
- Prioritized interrupt reporting
- Overrun, parity, and framing error detection

The COM1 Port at the CM6 has a RS232 compliant driver and the COM2 Port a RS422/485 compliant driver. The RS422/485 driver outputs can be controlled by a driver enable signal from the CPLD Control Register (CR) bit 0.

Ethernet Interface

The MPC8641 provides four Ethernet controllers; two of them are used in the CM6. Each channel has a reduced Gigabit Media Independent Interface (RGMII) interface to communicate with the Gigabit Phy MV88E1118. The two physical interface controllers provide the 10/100/1000 Base-T Ethernet to rear cPCI_J2 connector.

For registration and identification of a workstation in a LAN, a unique Network Interface Card (NIC) number is required. The NIC address is located in the SPD EEPROM.

General Purpose I/O

The CM6 provides 8 general purpose I/Os which are optional available at the rear cPCI_J2 connector. The GPIOs are controlled by the two PCIe/PCI bridges.

Interrupt Circuitry

The MPC8641 has an internal Programmable Interrupt Controller (PIC) which supports the following interrupt sources:

- External—Off-chip signals, IRQ[0:11] see chapter xxx for CM6 connection
- Internal interrupt sources These are on-chip sources from peripheral logic within the integrated device signaling error conditions that need to be addressed by software.

Interrupts generated from within the PIC itself, which are as follows:
— Global timers A and B internal to the PIC
— Interprocessor interrupts (IPI)—Intended for communication between different processor cores on the same device. (Can be used for self-interrupt in single-core devices)
— Message registers—From within the PIC. Triggered on register write, cleared on read. Used for interprocessor communication.
— Message-shared registers—From within the PIC. Triggered on register write, cleared on read. Used for cross-program communication.
— Four 32-bit message interrupt channels.
— Two groups of four global 32-bit timers clocked with the MPX clock or the RTC (25MHz) input. Timers within each group can be concatenated to time longer durations.

COP Debug Interface

The CM6 provides the COP debug interface signals to rear connector cPCI_J2. The COP signals are driven 3.3 V. The transition module CTM19 provides a compliant header for easy connection to a COP debug tool.

Note:
For correct operation of the COP interface at the CTM19 it is mandatory that the CTM19 is supplied with 3.3 V power.

JTAG Interface

The CM6 provides an IEEE 1149.1 (JTAG) Scan chain that can be used to check major components included in the chain for open and short circuits, and continuity. The JTAG Scan chain is driven at +3.3 V. The Boundary Scan chain for CM6 includes the following components:

- PI7C9X110 PCIe/PCI Bridge for cPCI
- PI7C9X130 PCIe/PCI Bridge for PMC
- MV88E1118 Giga Phy A

• MV88E1118 Giga Phy B
• PMC Slot
For more information please call GE Intelligent Platforms

Temperature

One National Semiconductor LM86 temperature sensor is implemented on the CM6 board. The sensor is located close to the CPU and shows the die-temperature of the CPU and the local onboard temperature. The sensor has two programmable over-temperature outputs integrated, which is used to protect the CPU for overheating.

The first stage is not used in the current CM6 implementation, the second stage is programmed to 110°C die temperature or 95°C board temperature if this temperature is reached the core voltage is switched off. The limit may be reprogrammed to user defined values.
If the CPU core power is switched-off by the temperature limit the board can only be re-powered with a reset switch actuation or a power-off/on cycle.

SMBus devices

The CM6 uses the two serial two-wire I^2C busses controlled by MPC8641 to communicate with several onboard devices:

I2C Bus #1

Device	Designator	SMBus address
Non-volatile digital switch	U1106	1010 111Xb

I2C Bus #2:

Table 21: SMBus devices

Device	Designator	SMBus address
Clock synthesizer *	U1000	1101 001Xb
SPD EEprom *	U1981	1010 000Xb
Factory EEprom *	U1981	1010 001Xb
User EEprom	U1983	1010 01nXb
Temperature sensor LM86	U1982	1001 100Xb

Devices marked by * are handled by the boot loader. It is strongly recommended not to access these devices under user software.

An 'X' at bit 0 represents the R/#W bit and 'n' a random address bit.

Serial EEPROMs

For storage of SPD and factory user data a serial EEPROM is implemented on the CM6 board. It is a standard 24C04 type EEPROM with 512 bytes. The user EEPROM is a 24C1024 type with 128 kByte.

Digital Switch

The CM6 has a digital switch for select and hold reset configurations. This digital switch is a Maxim DS3905 “Triple 128-Position Nonvolatile Digital Variable Resistor/Switch”. The settings of the digital switches are controlled by the boot loader.

Digital switch output 0 controls the “Core 1 Low Memory Offset Mode” which provides the capability for access to the lowest 256Mbyte of real addresses from core 1 to be offset in order to provide each core a unique and private address space in actual memory. The feature is used for Asymmetric Multi Processor (ASMP) operating systems.

Output 0:	open	- no extra translation performed
	set to 1kΩ	- extra 256 MByte translation

Digital switch output 1 controls the “Core 1 Enable” option
which allows the user to enable or disable the second core (if available) during power-on reset.

Output 1:	open	- Core 1 enabled
	set to 1kΩ	- Core 1 disabled

Digital switch output 2 is not used

LED

There is one status LED at the CM6 available and a status signal (BFAIL#) at the rear which is designated as an external “Board Fail” LED.

BFAIL# (cPCI J2 pin E19) is an open drain signal to source a LED at 3.3 V with 4 mA. The CM6 has an active low board fail signal (BFAIL#) at J2. The signal is active after reset and may set inactive after BIT test. The user may connect a red LED at the signal and if the LED is off this indicate a successful BIT test. BFAIL# is controlled with the CPLD Control Register (CR) Bit 6.

Table 22: Rear I/O LED indication

Status	BFAIL#
Power-up	default low
OS boot	see programming manual
User	Low or High

The Boot and Status LED (see table 23) is a green/red bi-color LED located at the board for boot up status indication. After boot loading the user software is free to use this LED for any purpose. The red and green of the bi-color LED is controlled at the CPLD Control Register (CR) Bit 4 and bit 5.

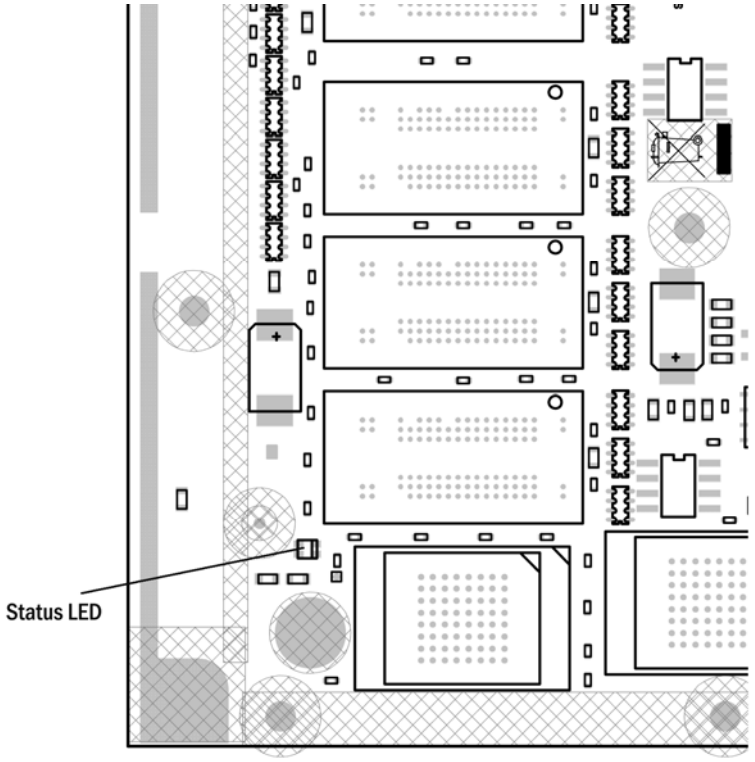

Figure 9: LED

Table 23: Boot and Status LED indication

Status	LED color
+3.3 V stable but at least one internal voltage missing	Red on
Power-up, still Reset state	Amber on
System Status – board is running	Green on
User status	Red/green/amber

Reset

The reset logic is controlled by the CPLD. The reset logic monitors all voltage and reset sources and only if all internal voltages are above a minimum level and all reset sources inactive the reset is released and the CPU may start with code execution. The reset source is monitored by the Reset Source Register (RSR) within the CPLD see section CPLD registers for description.

The following table lists all possible sources of reset.

Table 24: Reset sources

Source	Description
Power Monitor	All voltages are monitored and if one voltage is below the minimum requirement the CM6 is hold in reset.
Reset Button	External reset button connected at PRST# (cPCI-J2 pin C17). A low signal will issue a board reset. The PRST# is also active if the CM6 is in peripheral mode this deviants from the cPCI specification.
Reset from COP Interface	The board can be reset from the COP debug tool via COP_HRST# (cPCI-J2 pin E16).
Host Reset	The CPU may request a reset, signal is controlled by software.
Watchdog Reset	If the two stage watchdog time is elapsed the watchdog requests a reset.
PMC Reset	A Non-Monarch PMC (monarch is not supported) processor board may hold the CM6 and all subsystems in reset if this signal is active (RSTOUT# at PMC_Jn2 pin 59).
cPCI Reset	The compact PCI reset (cPI_J1 pin C5) is a bi-directional signal. In system mode the signal is the output of the internal reset and the reset source for all peripheral boards and subsystems at the cPCI system. In non-system mode it is an input and holds the CM6 (as cPCI peripheral) in reset.

CHAPTER 7 Specifications

PCB

FR4 Multilayer
UL V94-0

Size

Total board size: 3U, 4 HP

Dimensions

PCB: 100 mm x 178 mm x 20 mm

Weight

commercial style	460 g
conduction cooled style	480 g

Voltage Requirements

The CM6 requires +5 V and +3.3 V power. To avoid power sequencing problems the two power rails are controlled by MOSFET power switches. The internal power is switched on when the +5 V and +3.3 V reach the minimum voltage and the cPCI signal BDSEL# (cPCI-J1 pin D15) is low. The MOSFET power control limits also the in-rush current for the +5 V and +3.3 V. All other internal voltages are derived from +3.3 V and 5.0 V and are controlled internal for correct sequencing.
+12 V and -12 V are not required except if the PMC requires these voltages or the “Flash Kill” option (+12V) is provided. +12V and -12V voltages are not sequencing controlled.

Table 25: Voltage Requirements

Voltage	Min	Max
+3.3 V	3,20 V (3,135 V *)	3,46 V
+5 V	4,85 V (4,750 V *)	5,25 V
+12 V	11,4 V	+12,6 V
-12 V	-12,6 V	-11,4 V

Note
*: if one voltage is below these values the MOSFETs in the +5 V and 3.3 V power rail will switch off

Attention:

Do not insert a CM6 board in a 3/6U 64-bit Backplane because this may damage electrical interfaces at the CM6.

Power Consumption

Table 26 is intended to help you calculate the power consumption of a CM6 system. For measurement, the CM6 board is mounted on a CPCI backplane. The values are typical measured**.**

Table 26: Power consumption

CM6	VxWorks prompt, both Ethernet Giga Link, mid-range temperature		Memory Test program, CPU and memory running at max. CPU die temperature, both Ethernet Gigabit Link	
	+5 V	+3.3 V	+5 V	+3.3 V
CM6 Single 1000MHz DDR400/1 GB	11 W	13 W	12 W	15 W
CM6 Dual 1000MHz DDR400/1 GB	19 W	13 W	21 W	15 W
CM6 Dual 1333MHz/DDR533/1 GB	23 W	14 W	25 W	16 W
CM6 Dual 1000MHz low voltage DDR500/ 1 GB	14 W	14 W	15 W	16 W

Table 7: Flash Kill Power Consumption

	+12 V
CM6 when Flash Kill active	8 A (approximately 0.5 second)

Environment Conditions

Ambient temperatures and humidity values for the CM6:

Table 27: Temperature and humidity conditions

	1-, 2-Style	3-, 4-, 8-Style
High Temperature		
- Storage (see note below)	+85 °C	+85 °C
- Operating (see Figure 9)		
Low Temperature		
- Storage (see note below)	-40 °C	-40 °C
- Operating	0 °C	-40 °C
Temperature Shock		
- Storage	+/-10 °C/min	+/-20 °C/min
- Operating	+/-5 °C/min	+/-10 °C/min
Relative Humidity		
- Storage, Operating	Up to 95 %, non-condensing	

Storage temperature for N-, 8-styles is between -55 °C (low) & +105 °C (high).

Shock and vibration (see table 28) values for the CM6:

Table 28: Shock and vibration conditions

	1-, 2-, 3-, 4-Style
Vibration	
- Spectrum	5 to 100 Hz
- Acceleration	2 g_{rms}
Shock	
- Amplitude	12 g
- Duration	6 ms

Table 29: Shock and vibration conditions

	8-Style	
Vibration		
- Spectrum	5 Hz - 2000 Hz	
- Acceleration	14 g_{rms}	
Shock		
- Amplitude	40 g	100 g
- Duration	11 ms	6 ms

For highest operating temperatures for air cooled styles please refer to the following diagram:

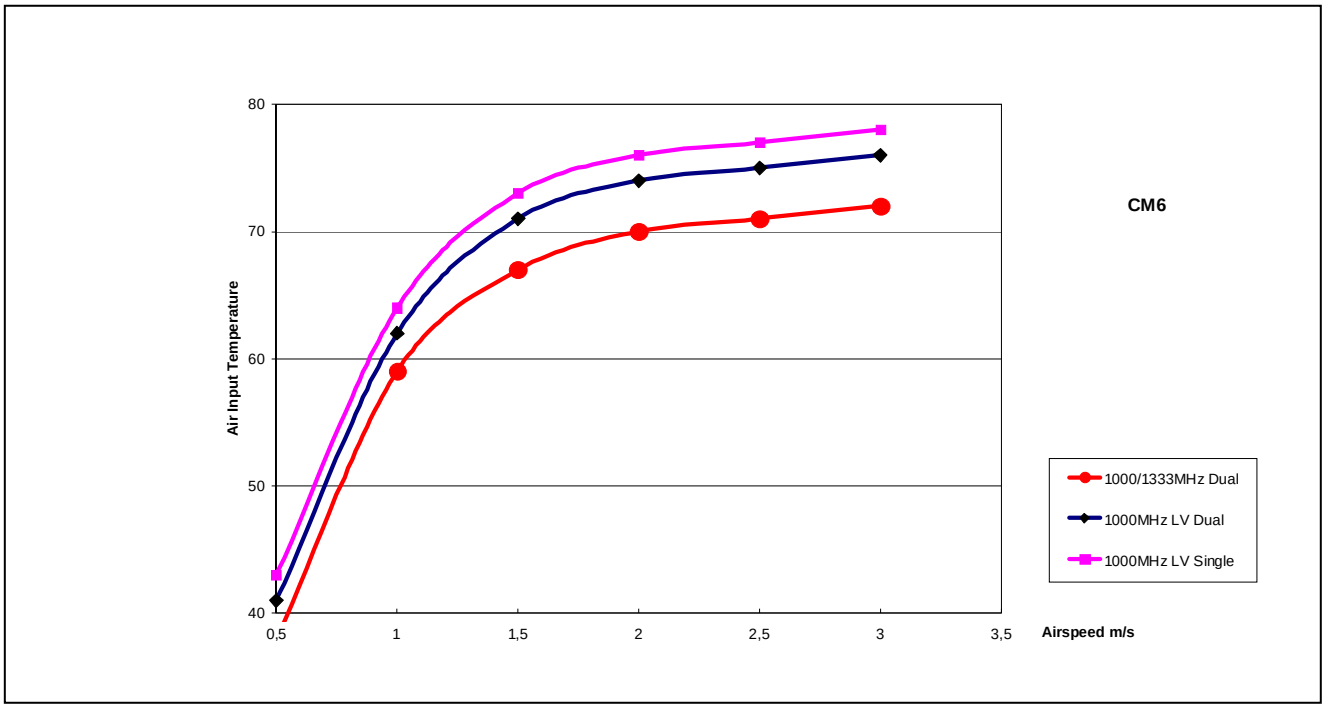

Figure 10: Heat sink diagram for air cooled versions (1-,2-,3-,4-style)

- diagram is for typical power consumption, with both Gigabit links up and without a mounted PMC card
- 0 m/s airflow means convection cooled only
- The core temperature of the CPU can be read out via the onboard temperature sensor. The value must be kept below 105 °C for all operating conditions. This value is already included in the airspeed diagram above.

Table 30: Maximal card edge temperature for conduction cooled version (8-style)

CM6	Maximal Card Edge Temperature
CM6 Dual 1000MHz DDR400/1 GB	73°C

- typical power consumption, with both Gigabit links up and without a mounted PMC card
- the maximal card edge is defined if CPU core temperature reaches 105°C
- please see CM6 thermal report for more information

Electrical Characteristics

General Purpose IO 0-7

The general purpose I/O pins can be programmed as inputs, with following signal input voltages:

Table 31: GPIO input signal voltages

Signal	Voltage
Vil	-0.5 V ... +0.8 V
Vih	+2.0 V ... VCC3 + 0.5 V
Iin	+/-10 µA

VCC3 is the +3.3 V voltage from the backplane

When programmed as outputs, the following signal levels are supplied.

Table 32: GPIO output voltage signal levels

Signal	Voltage
Vol	max. 0.4 V @ 4 mA sinking
Voh	min. VCC3-0.5 V @ -2 mA sourcing

VCC3 is the +3.3 V voltage from the backplane

The GPIOs are default inputs after reset. On the CM6 board there are 10kΩ pull-ups to +3.3 V at all GPIOs.

Note:
On CM6 Version 1.x only signals GPIO4...7 are usable.

COM1 RS232 Interface

The RS232 interface uses a Texas Instruments® MAX3243 RS232 Line Driver/Receiver chip with following electrical characteristics:

Table 33: COM1 electrical characteristics

Signal	Voltage
Maximum data rate	150 kbit/s
C_L = 1000 pF R_L=3 KΩ	
Vi (Receiver)	-25 V ... +25 V
Vo (Driver)	min +/- 5 V
VT+ (Receiver input threshold)	max +2.7 V
VT- (Receiver input threshold)	min -2.7 V

COM2 RS422/485 Interface

The RS422/485 interface uses the Maxim® MAX1484 Transceiver chip with following electrical characteristics:

Table 34: COM2 electrical characteristics

Signal	Voltage
Maximum data rate	12 Mbit/s
Vi (driver/receiver absolute maximum)	-8 V ... +12.5 V
Differential driver output (no load) Differential driver output (R=50 Ω RS422) Differential driver output (R=270 Ω RS485)	max 5 V min 2.0 V min 1.5 V
Driver output short current	min 35 mA, max 250 mA
Receiver differential threshold	min -200 mV, max 200 mV
Receiver hysteresis	typ 70 mV
Receiver input resistance	min 96 kΩ

Isolation

The Isolation of the Ethernet outputs is limited to 500 V peak against logic ground (GND) and any other supply voltage.

By itself the onboard logic ground (GND) and the front panel/chassis frame ground (FGND) are isolated on the CM6 with a layout distance of more than 0.3 mm in all PCB layers. Also standard racks (our starter cage, too) connect both grounds at the power supply for safety reasons.

Placement Plan Component Side CM6 V1

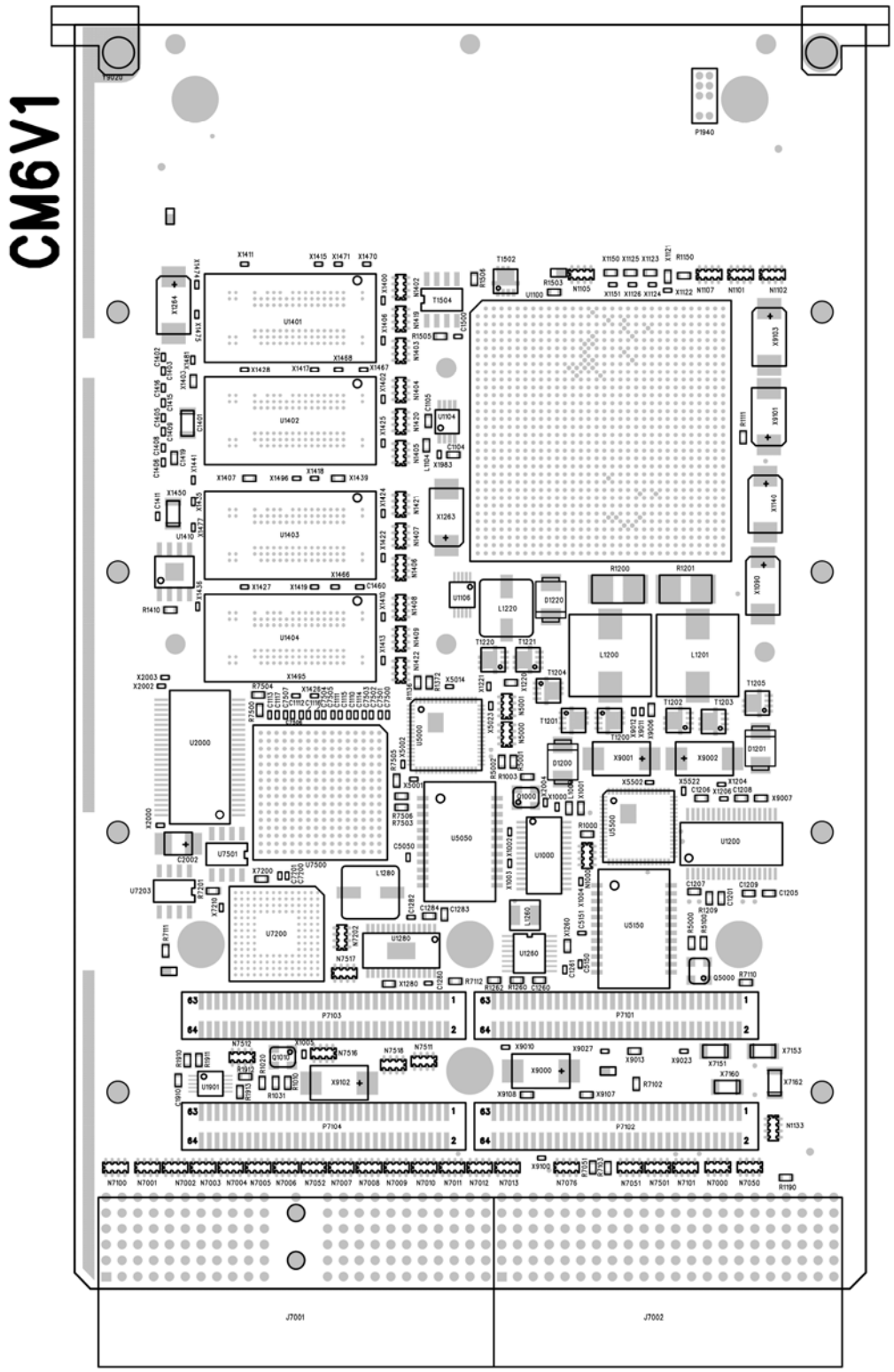

Figure 11: Placement diagram component side

Placement Plan Solder Side CM6 V1

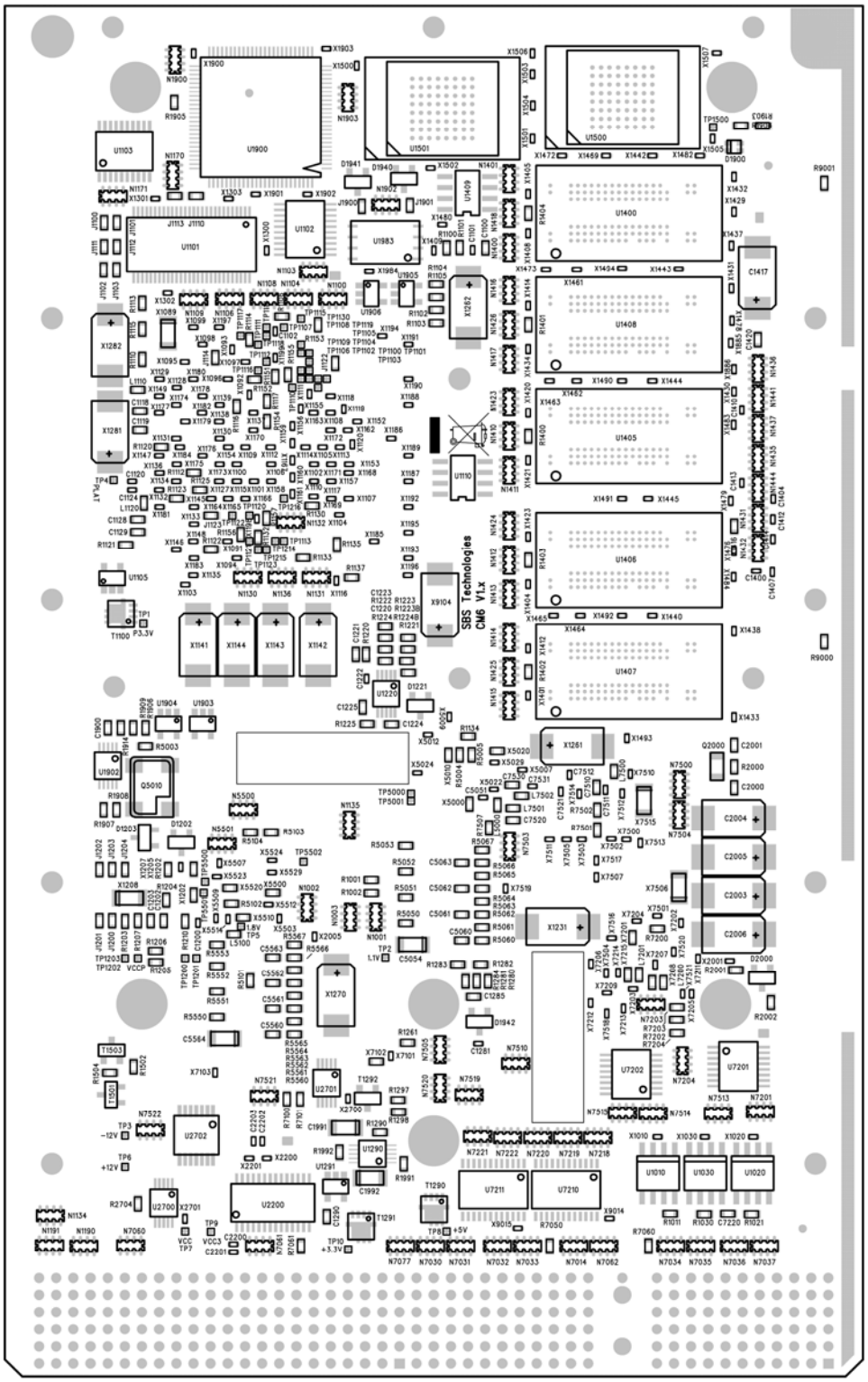

Figure 12: Placement diagram solder side

Appendix A Transition Module CTM19

The CTM19 transition module is used for easy connection of I/O signals to standard connectors.

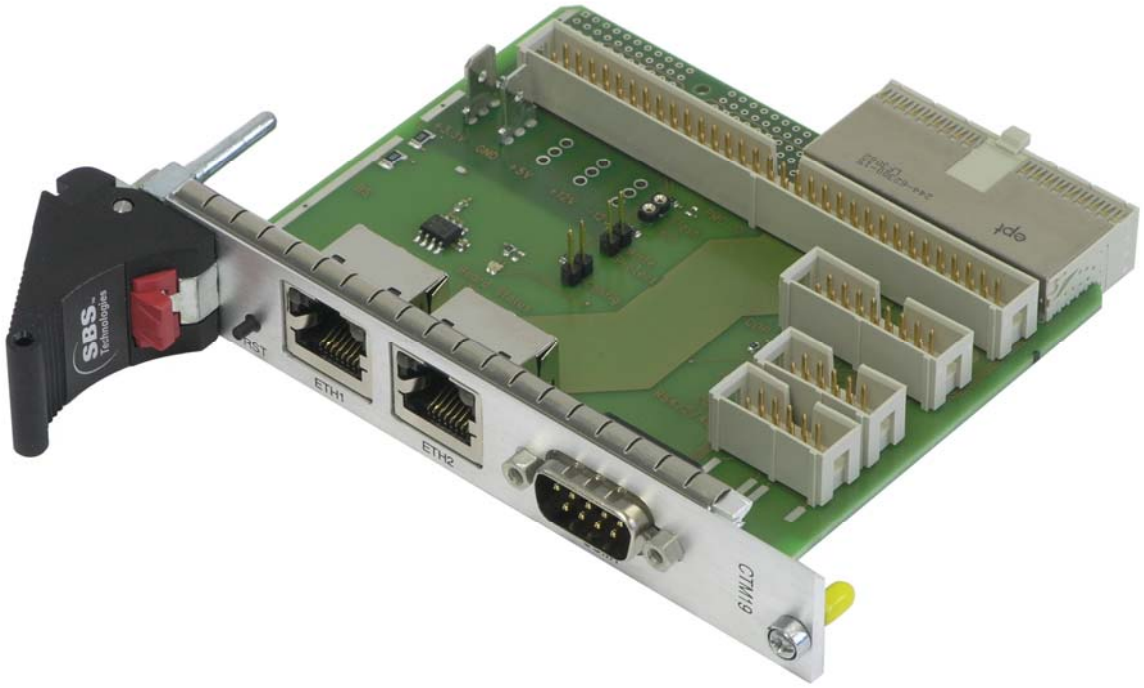

Figure 13: Transition Module CTM19

Please refer to the drawing for the location of available interfaces:

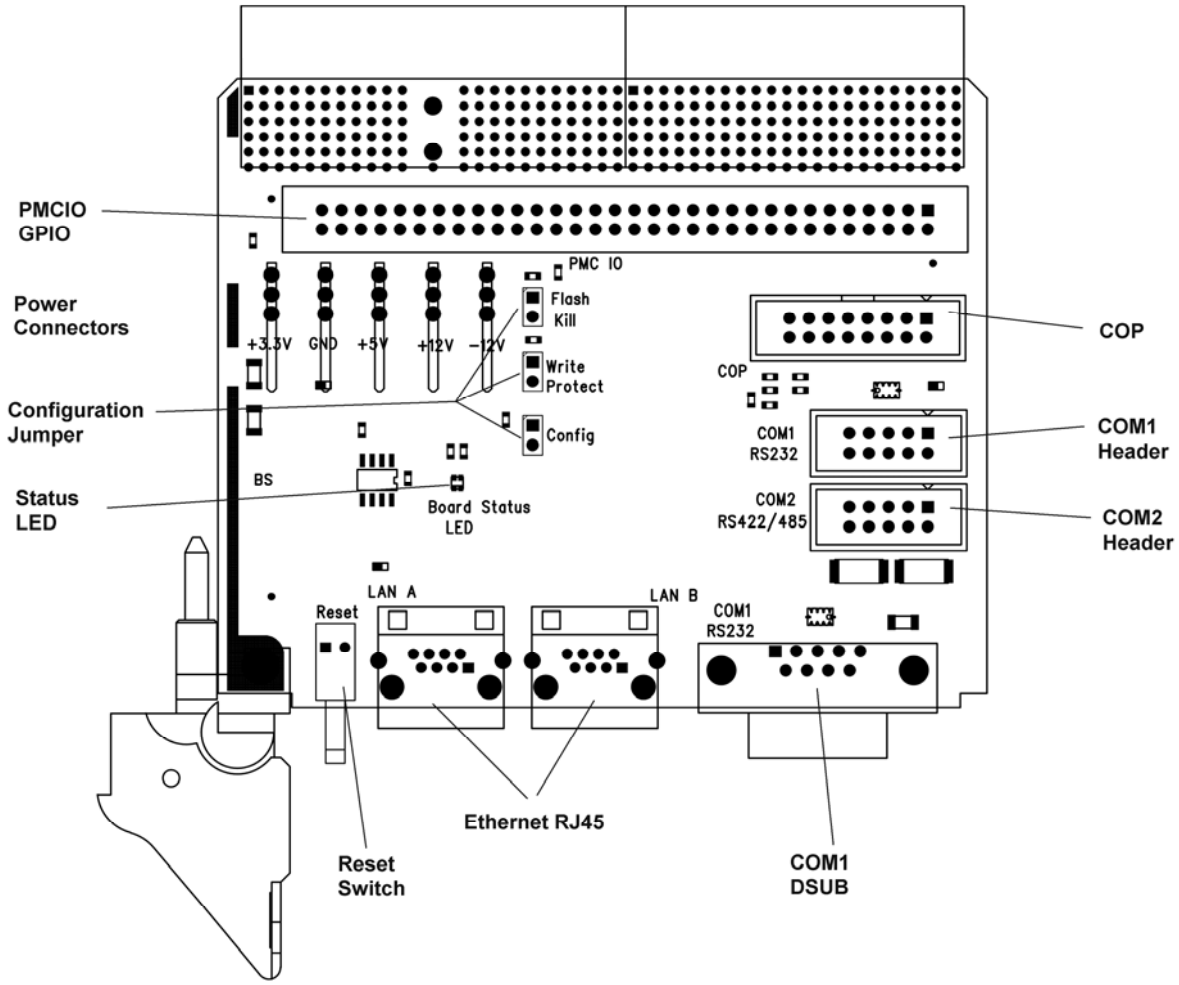

Figure 14: Layout of Transition Module

CTM19 Interfaces

This chapter describes all connector pin outs on the CTM19 transition module.

Serial Interfaces COM1 (P2200, P2202) and COM2 (P2201)

The CM6 offers two serial ports. COM1 is a RS232 compliant and COM2 has a RS422/RS485 interface. All COM ports are accessible via the transition module on 10-pin headers. COM1 is also available at the rear panel with a 9-pin D-sub connector.

For the COM2 signals there are provisions for termination resistors at the CTS and RXD signals.

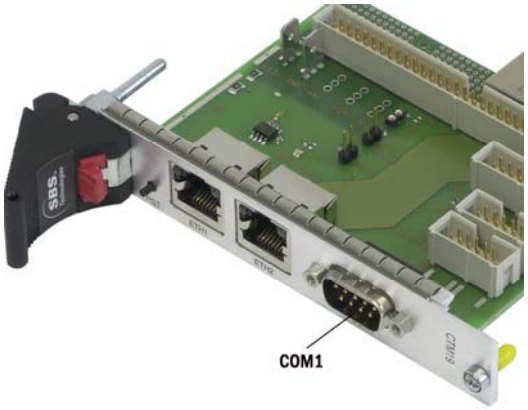

Figure 15: COM1 at Transition Module

Table 35: COM1 at Transition Module

Name RS232	COM2 P2203 9 pin D-Sub	P2200 pin header
DCD	1	1
DSR	6	2
RXD	2	3
RTS	7	4
TXD	3	5
CTS	8	6
DTR	4	7
RI	9	8
GND	5	9
+5 V fused [a]	-	10

[a] +5 V supply via P1101 of the CTM19 and fused with a 2 A fuse. The installed fuse does automatically recover if the over current is resolved.

Table 36: COM2 at Transition Module

Name RS422/485	P2200 pin header
TXD-	1
TXD+	2
RTS-	3
RTS+	4
CTS-	5
CTS+	6
RXD+	7
RXD-	8
GND	9
+5 V fused [a]	10

[a] +5 V supply via P1101 of the CTM19 and fused with a 2A fuse. The installed fuse does automatically recover if the over current is resolved.

COP Interface P1300

A 16pin header P1300 provides the COP debug interface for the PowerPC processor of the CM6.

Note

For proper operation of the COP interface the CTM19 must be supplied with +3.3 V via the P1102 power connector.

Table 37: COP debug interface (P1300)

COP Interface	P1300	Remarks
COP_TDO	1	
	2	
COP_TDI	3	
COP_TRST#	4	
COPVCC3	5	3.3 V supplied via P1102 and 4.7 kΩ resistor
COPVCC3	6	3.3 V supplied via P1102 and 10 Ω resistor for current limitation
COP_TCK	7	
CKSTOPIN#	8	
COP_TMS	9	
-	10	
COP_SRST#	11	
GND	12	
COP_HRST#	13	
Key	14	
CHKSTOPOUT#	15	
GND	16	

Ethernet connectors P5000, P5500

The both Ethernet RJ45 8-pin connectors mounted at the module's front panel are capable for Gigabit Ethernet. Gigabit Ethernet consists of 4 transmit/receive signal pairs. The table shows also the transmit and receive signals if the interface is working in 10BaseT or 100BaseTX mode.

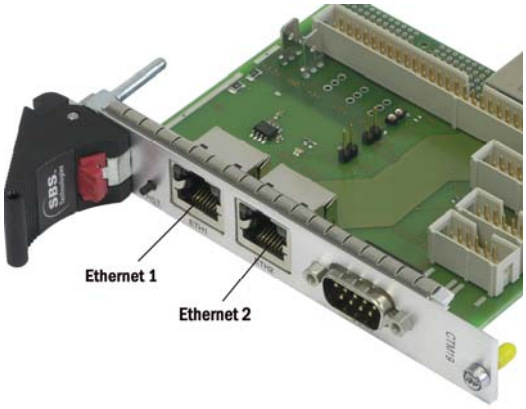

Figure 16: Ethernet connectors

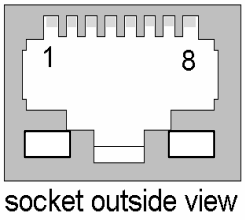

Figure 17: RJ45 Ethernet connectors

The LEDs at the RJ45 connectors are not connected and have no function.

Table 38: Ethernet pin assignments (P5000 & P5500)

Name	**Ethernet1** P5000 **Ethernet2** P5500
LPx_DA+ (TxD+)	1
LPx_DA- (TxD-)	2
LPx_DB+ (RxD+)	3
LPx_DC+	4
LPx_DC-	5
LPx_DB- (RxD-)	6
LPx_DD+	7
LPx_DD-	8
FGND	

Configuration jumpers J1900, J1901, J1902

Software Configuration Jumper J1900

If the software configuration jumper J1900 is closed the software can execute other boot code. Please refer to the programming manual for exact operation.

Write Protect Jumper J1901

If the Write Protect jumper J1901 is closed all write commands to the Flash and nvSRAM/RTC devices are disabled.

Flash Kill Option J1902

For security reasons the flash devices can be destroyed with this optional feature. If the Flash Kill jumper (J1902) is closed and the option is available at the CM6 this will destroy the flash devices.

PMCIO connector P7101

P7101 a 64 pin header contains PMCIO signals:

Table 39: Miscellaneous connector P8100

Name	P7101		Name
PMCIO01/GPIO0 *	1	2	PMCIO02/GPIO1*
PMCIO03/GPIO2 *	3	4	PMCIO04/GPIO3*
PMCIO05/GPIO4 *	5	6	PMCIO06/GPIO5*
PMCIO07/GPIO6 *	7	8	PMCIO07/GPIO7*
PMCIO09/FKILL# *	9	10	PMCIO10
PMCIO11	11	12	PMCIO12
PMCIO13	13	14	PMCIO14
PMCIO15	15	16	PMCIO16
PMCIO17	17	18	PMCIO18
PMCIO19	19	20	PMCIO20
PMCIO21	21	22	PMCIO22
PMCIO23	23	24	PMCIO24
PMCIO25	25	26	PMCIO26/52*
PMCIO27	27	28	PMCIO28
PMCIO29	29	30	PMCIO30/37*
PMCIO31	31	32	PMCI32/39
	33	34	
	35	36	PMCIO36/42*
PMCIO30/37*	37	38	PMCIO38/44*
PMCIO32/39*	39	40	
	41	42	PMCIO36/42
	43	44	
	45	46	
	47	48	
	49	50	PMCIO50
	51	52	PMCIO26/52*
	53	54	
	55	56	
	57	58	
	59	60	
	61	62	
HW_\CFG	63	64	HW_\WP

*: Alternative signal assignment depends from CM6 option.

Board Status LED

A red Board Status LED is used at CTM19 and drives a LED with following meaning:

Table 40: Board Fail LED at CTM19

Status	LED color
Power-up	Red on
OS boot	see programming manual
User	Red on or off

Note:
For proper operation of the LED the CTM19 must be supplied with +3.3 V via the P1102 power connector.

Reset Button

The Reset button will issue a hard power-on reset. The reset signal PRST# is active for all subsystems of the CM6 and if the CM6 board is system board also for all peripheral boards at the cPCI system.

Power connectors P1100, P1101, P1102

These power connectors are only optionally mounted except P1102 (+3.3 V for the LED and COP interface) to power the CM6 without a backplane.

P1100 GND
P1101 +5 V
P1102 +3.3 V
P1103 +12 V
P1104 -12 V

cPCI connectors P1001, P1002

The cPCI connector P1002 provides the CM6 rear I/O signals. The cPCI connector P1001 is only optionally mounted to power the CM6 without a backplane in conjunction with the power connectors P1100…P1104. In this case VIO is connected to 3.3 V at the CTM19.

J1002	A	B	C	D	E	F
22						GND
21		GND	COP_TDI	SW_CFG#	HW_WP#	GND
20		GND	COP_TMS	COP_TRST#	COP_TCK	GND
19	GND	GND	CKSTPIN#	CKSTPOUT	BFAIL#	GND
18	PMCIO03/GPIO2	PMCIO02/GPIO1	PMCIO01/GPIO0	COP_TDO	COP_SRST#	GND
17	PMCIO05/GPIO4	PMCIO04/GPIO3	PRST#			GND
16	PMCIO06/GPIO5	PMCIO06/GPIO5		GND	COP_HRST#	GND
15	PMCIO09/FKILL#	PMCIO08/GPIO7				GND
14	PMCIO12	PMCIO11	PMCIO10	C1_RXD	C1_RTS	GND
13	PMCIO15	PMCIO14	PMCIO13	C1_TXD	C2_RTS+	GND
12	PMCIO18	PMCIO17	PMCIO16	C1_CTS	C2_RTS-	GND
11	PMCIO21	PMCIO20	PMCIO19	LPB_DA+	LPB_DB+	GND
10	PMCIO24	PMCIO23	PMCIO22	LPB_DA-	LPB_DB-	GND
9	PMCIO26/52	PMCIO25	C2_CTS+	LPB_DC+	LPB_DD+	GND
8	PMCIO28	PMCIO27	C2_CTS-	LPB_DC-	LPB_DD-	GND
7	PMCIO30/37	PMCIO29	C2_TXD+	LPA_DB+	LPA_DA+	GND
6	PMCIO32/39	PMCIO31	C2_TXD-	LPA_DB-	LPA_DA-	GND
5	PMCIO38/44	PMCIO36/42	C2_RXD+	LPA_DD+	LPA_DC+	GND
4		PMCIO50	C2_RXD-	LPA_DD-	LPA_DC-	GND
3		GND				GND
2			PDN [b]			GND
1		GND				GND
J1001	A	B	C	D	E	F
25	+5 V			+3.3 V	+5 V	GND
24		+5 V	VIO [a]			GND
23	+3.3 V			+5 V		GND
22		GND	+3.3 V			GND
21	+3.3 V					GND
20			VIO [a]			GND
19	+3.3 V			GND		GND
18		GND	+3.3 V			GND
17	+3.3 V			GND		GND
16			VIO [a]			GND
15	+3.3 V			GND(BDSEL#)		GND
12-14	KEY	KEY	KEY	KEY	KEY	KEY
11				GND		GND
10		GND	+3.3 V			GND
9				GND		GND
8		GND	VIO [a]			GND
7				GND		GND
6			+3.3 V			GND
5				GND		GND
4			VIO [a]			GND
3				+5 V		GND
2		+5 V				GND
1	+5 V	-12V		+12V	+5 V	GND

[a] VIO is connected to +3.3V
[b] optionally 100 Ω pull-down if the CTM19 is used without backplane

Placement Plan CTM19

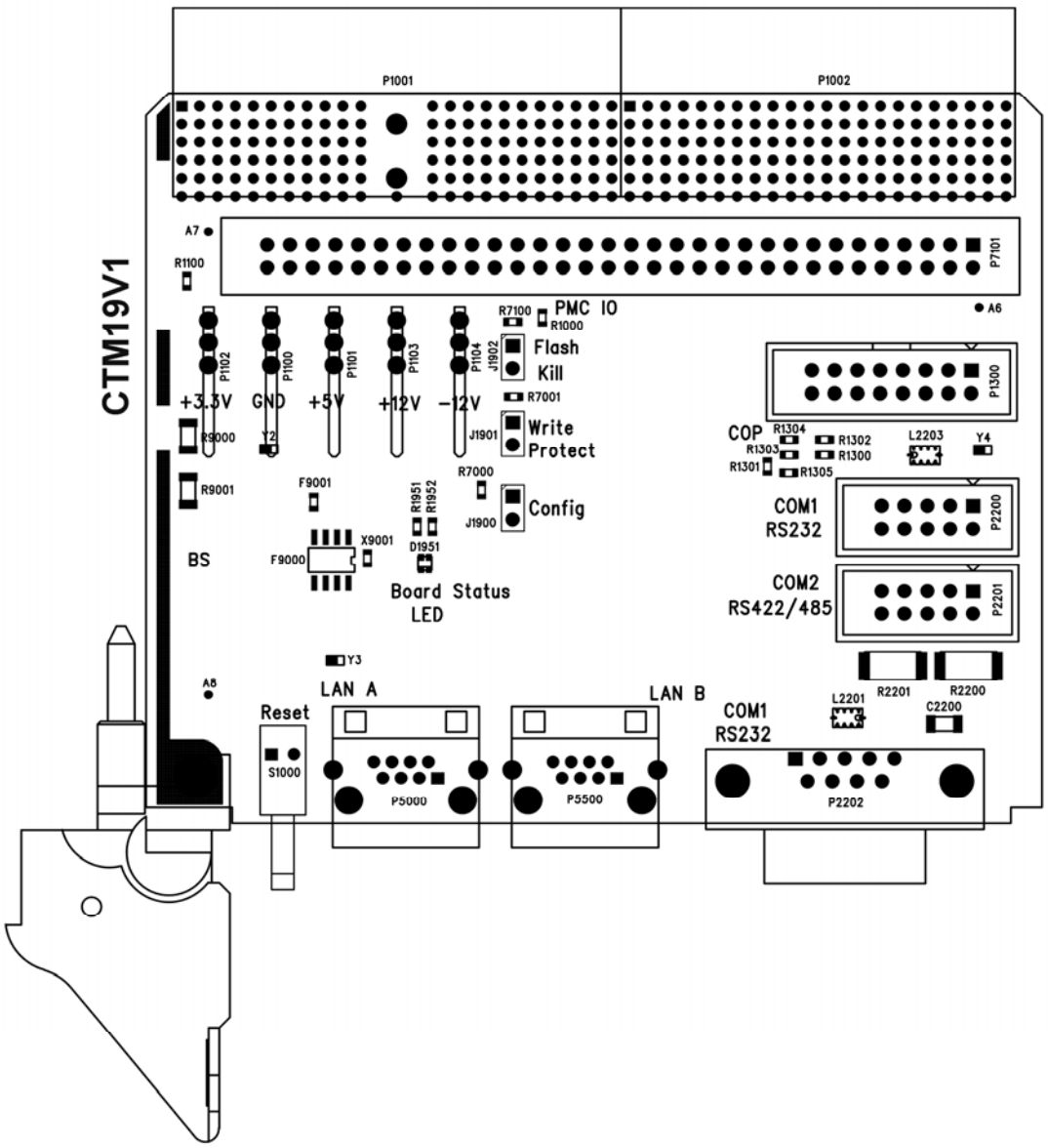

Figure 18: Placement plan CTM19

Appendix B Support, Service and Warranty

Chapter Scope

The following sections describes GE Intelligent Platforms' product support program. It states our product warranty terms and provides details about what action to take if you experience a problem with the product.

Geographical Regions

World-wide headquarter of GE Intelligent Platforms, Inc. is at

GE Intelligent Platforms Inc.
2500 Austin Drive
Charlottesville, VA 22911
U.S.A.

Web: http://www.ge-ip.com

GE Intelligent Platforms, Inc. uses two regional headquarters for the purpose of support, service, RMA returns and other functions.

Regional areas:

WW	world-wide
EU	Germany: Augsburg UK: Towcester
US	Americas & Pacific Rim (Japan, Korea, China, Philippines, AUS, NZ)

Technical Support

If you should have a problem with a GE Intelligent Platforms product: Free technical support is available by phone, fax or email. Telephone support is available at main locations or at the regional center where the product was bought.

Germany	US
Monday through Thursday 8:00 – 17:00 (CET) Friday 8:00 – 16:00 (CET) Phone +49-821-5034-170 Fax +49-821-5034-119 E-Mail: support.augsburg.ip@ge.com	Monday through Friday 8:30 AM – 5:30 PM (Eastern Time) Phone +1-800-322-3616 Fax +1- E-Mail: support.huntsville.ip@ge.com

Support on the Web

For support and information, visit our website at
http://www.ge-ip.com/

Information for components, corresponding driver software, etc. can also be found at the following locations:

AMD Corp.	www.amd.com
American Megatrends	www.ami.com
Fedora	www.fedora.redhat.com
IBM Corp.	www.ibm.com
Intel Corp.	www.intel.com
Linear Technology	www.linear-tech.com
Microsoft Corp.	www.microsoft.com
Freescale Corp.	www.freescale.com
Novell	www.novell.com
NVIDIA	www.nvidia.com
Pericom	www.pericom.com
PCI Industrial Computer Manufacturing Group	www.picmg.org
PLX Technology	www.plxtech.com
QNX Software Systems	www.qnx.com
Red Hat	www.redhat.com
Symbios Logic	www.lsilogic.com
VITA	www.vita.com
Wind River Systems	www.windriver.com

Warranty

For detailed warranty information, visit our website at
http://www.ge-ip.com

Error Report

For error reports and RMA (Return Material Authorization) forms contact support at these email addresses:
repairs.augsburg.ip@ge.com
repairs.huntsville.ip@ge.com

In case of difficulties provide at least the information listed below to an appropriate support center or on their web site as listed above.

- RMA Number, if applicable
- Product & Serial Number
- Part Number
- Version
- Bios built date [a]
- Contact: Name & Phone Number
- Detailed Description of the Problem/Defect

For PowerPC based computers include:

- Bootload version
- Operating system used
- Version of the BSP (Board Support Package)

GE Intelligent Platforms Information Centers

Americas:
1 800 322 3616 or 1 256 880 0444

Asia Pacific:
86 10 6561 1561

Europe, Middle East and Africa:
Germany +49 821 5034-0
UK +44 1327 359444

Additional Resources

For more information, please visit the GE Intelligent Platforms Embedded Systems web site at:

www.ge-ip.com

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